PAMS Technical Documentation

NSE–6 Series Transceivers

Disassembly & Troubleshooting Instructions

Original 08/98

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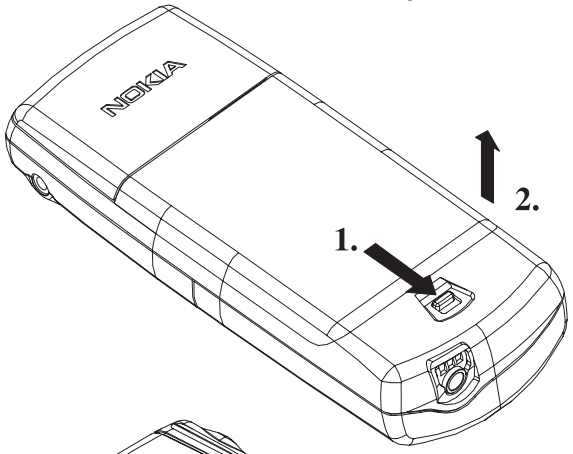
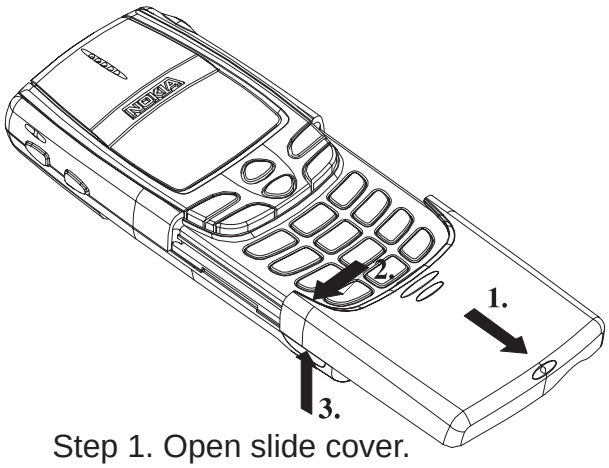
Disassembly

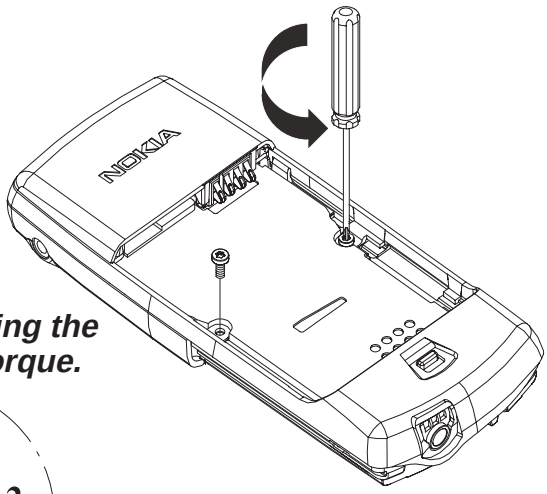
Remove battery





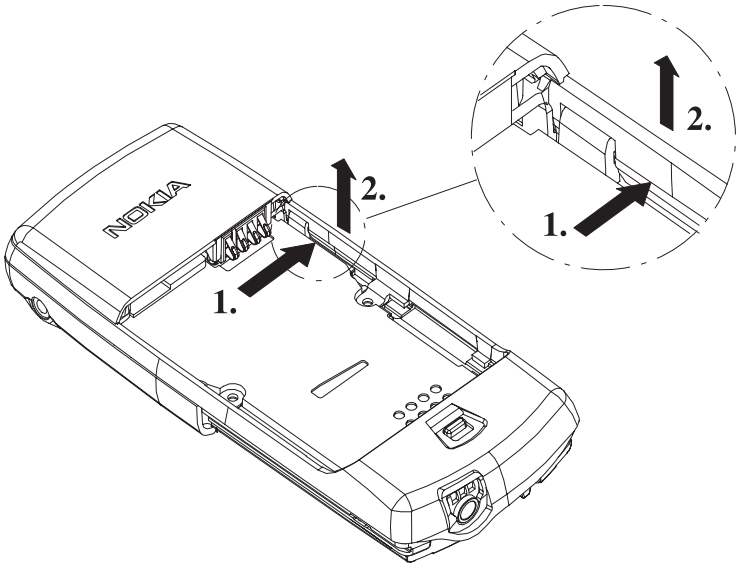
Step 1. Open slide cover.
Step 2. Push slide edge outwards.
Step 3. Lift slide up from the edge and slide will be released.

Remove a–cover screws (2 pcs)

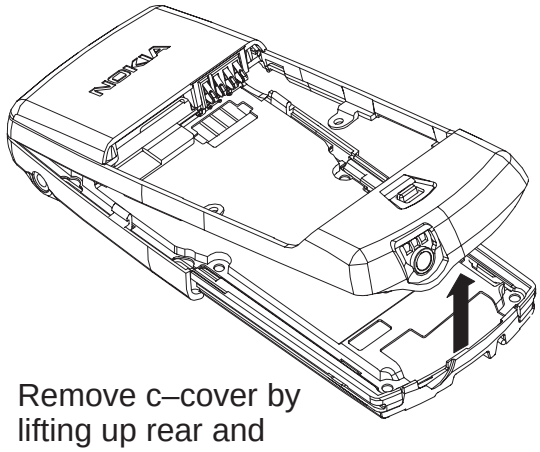


NOTE: When assembling the screws, use 17 Ncm torque.

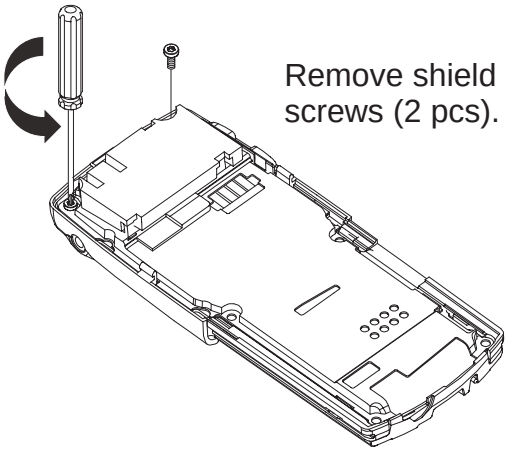
Turn the phone around and remove C–cover screws (2 pcs)



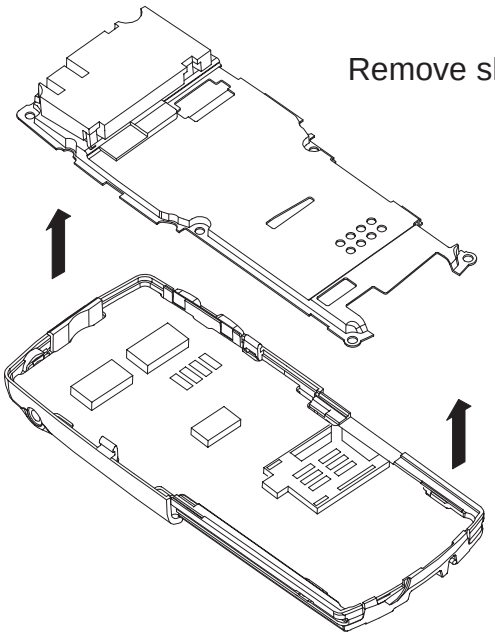
Step 1. Push c–cover edge outwards to release it behind locking snap
Step 2. Lift up the edge to release c–cover.
Step 3. Repeat the operation on both sides.



Remove c–cover by lifting up rear and pulling cover out.

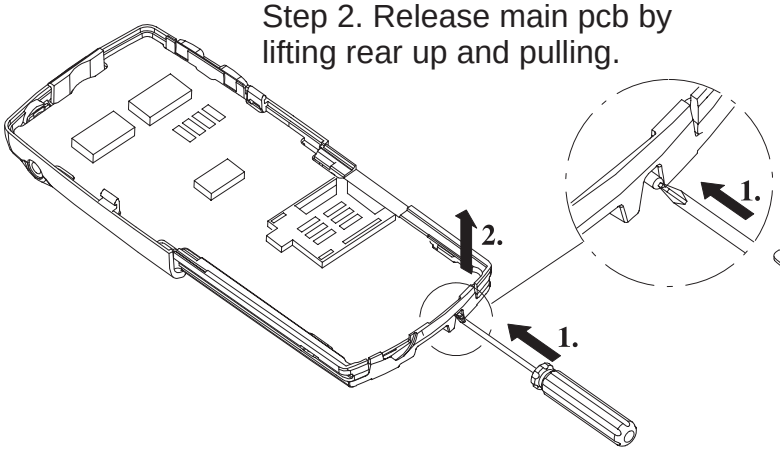


Remove shield screws (2 pcs).

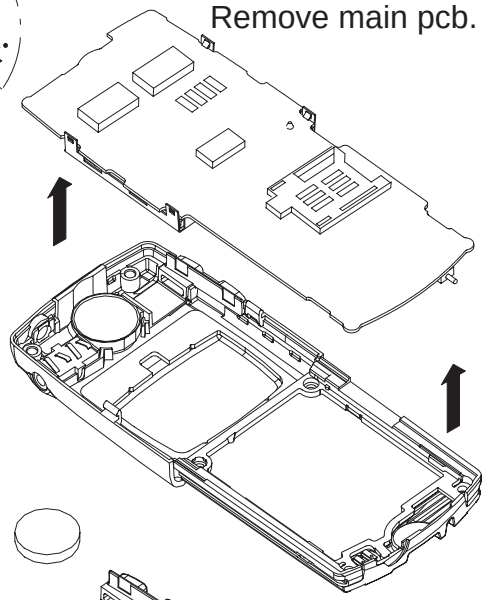


Remove shield.

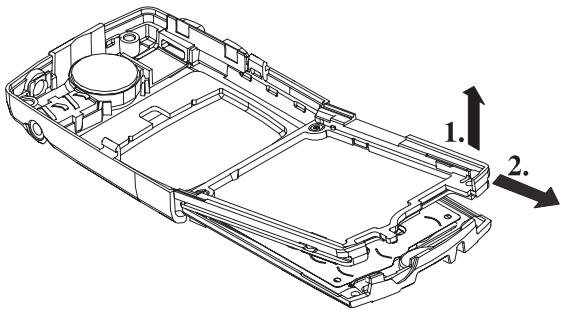
Step 1. Push slide detector switch to the bottom and hold.
Step 2. Release main pcb by lifting rear up and pulling.

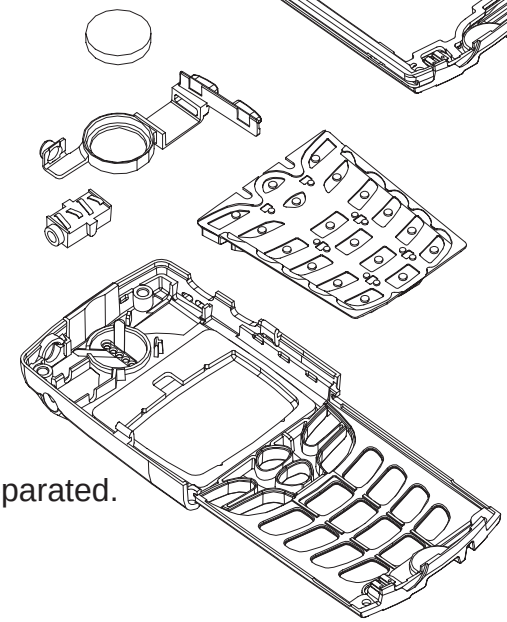


Remove main pcb.



Step 1. Lift slide frame from bottom and loosen it from a–cover.
Step 2. Remove slide frame, UI–board will follow.





Parts can be separated.

Baseband Testing

The MCU software enters a local mode at start–up if suitable resistors are connected to the BTEMP and BSI lines. NOTE! Baseband doesn't wake up automatically when the battery voltage is connected. Power must be switched on via:

1. Pwr key or
2. BTEMP line or
3. Charger

In the local mode the baseband can be controlled through MBUS or FBUS connections by a PC–locals software. Baseband internal connections are tested with self tests if possible. By connecting MAD2 pin ROW5 to ground, MAD2 pins are toggled as a daisy chain, which can be used for detecting short circuits in MAD2 pins. Test pads are placed on engine pcb for service and production troubleshooting purposes in some supply voltage and signal lines.

Alignments

Within alignment those parameters are adjusted, that cannot be set accurate enough by design because of component tolerances. Due to use of 5% resistor values, the channels of the CCONT A/D converters need to be aligned in the production phase. Within battery voltage tuning the MCU software reads the A/D reading from CCONT at 4.1V and stores this reading to EEPROM memory as a reference point. Another reference point is created by assuming that while the input voltage is zero, A/D reading is also zero. Now the slope is known and A/D readings can be calibrated. Calibration is included in VBAT A/D reading task.

Battery charging voltage VCHAR and current ICHAR are calibrated using one test setting. Test jig in production/service must have a connection to battery terminals. ICHAR and VCHAR are supplied fron the jig and service software calculates values, which are then stored to EEPROM.

Trouble Shooting

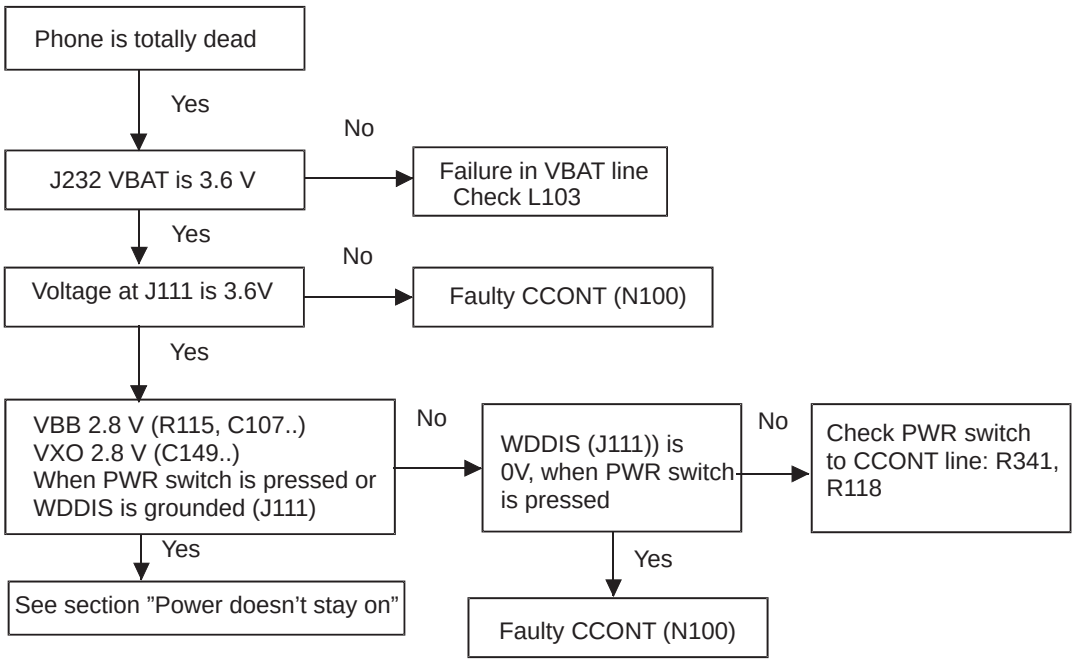
The following hints should facility finding the cause of the problem when the circuitry seems to be faulty. This trouble shooting instruction is divided following section.

1. Phone is totally dead
2. Flash programming doesn‘t work
3. Power doesn‘t stay on or the phone is jammed
4. Display information: Contact Service
5. Phone doesn‘t register to the network or phone doesn‘t make a call.
6. SIM card related failures (insert SIM card or card rejected).
7. Audio fault.
8. Charging fault

The first thing to do is carry out a thorough visual check of the module. Ensure in particular that:
a) there are not any mechanical damages
b) soldered joints are OK

Phone is totally dead

This means that the phone doesn't take current at all when the power switch is pressed or when the watchdog disable pin (X001 pin 11, J111) is grounded. Used battery voltage must be higher than 3.1 V. Otherwise the hardware of CCONT (N100) prevents totally power switch–on.



Flash programming doesn't work

The flash programming can be done via panel connector X001 or via dedicated PCB pads. In production, the first programming is done via panel connector. After this, the panel connector is cut away, thus the programming must be done via PCB pads visible through the shield under the battery. The main difference between these is that FLASH programming voltage is produced differently.

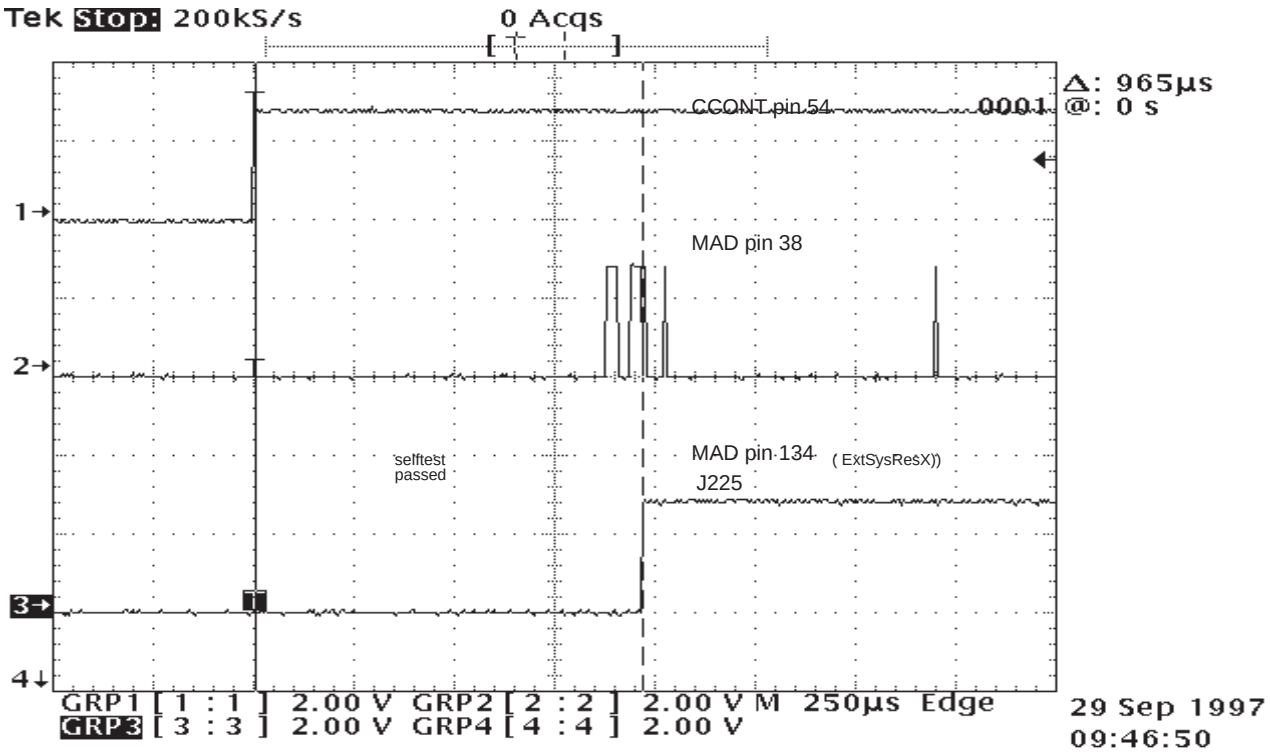
In flash programming error cases the flash prommer can give some information about a fault. The fault information messages could be:

– MCU doesn't boot
– Serial clock line failure
– Serial data line failure
– External RAM fault
– Algorithm file or alias ID don't find
– MCU flash Vpp error

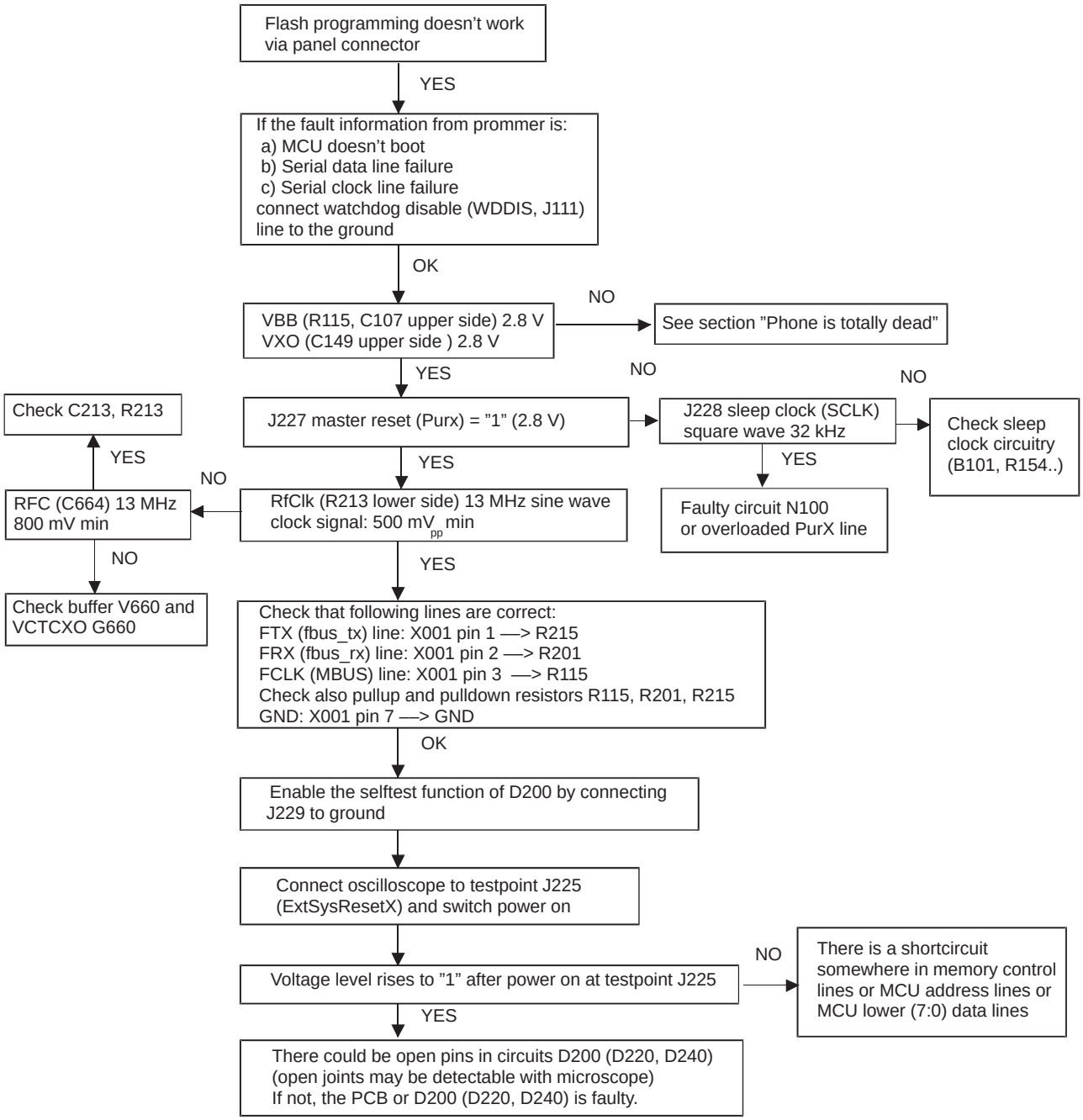
In cases of unsuccesful flash programming there is a possibility to check short circuits between the memories and the MCU (MAD2). It is useful to do this test, when the fault information is: MCU doesn't boot, Serial clock line failure or Serial data line failure. The test procedure is following:

1. Connect testpoint J229 to ground.
2. Switch the power on.
3. If the voltage level in testpoint J225 is 2.8 V ("1"), the interface is OK. If there is a short circuit, the voltage level in testpoint J225 stays low and 32kHz square wave signal can be seen in the lines which are already tested.

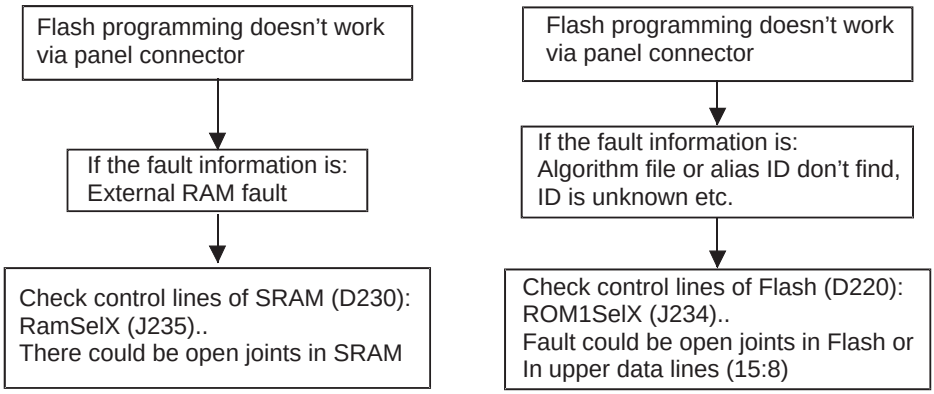
It must be remembered that this test can only find short circuits, not open pins. In addition upper data lines (15:8) of flash memory D220 are not included in this test.

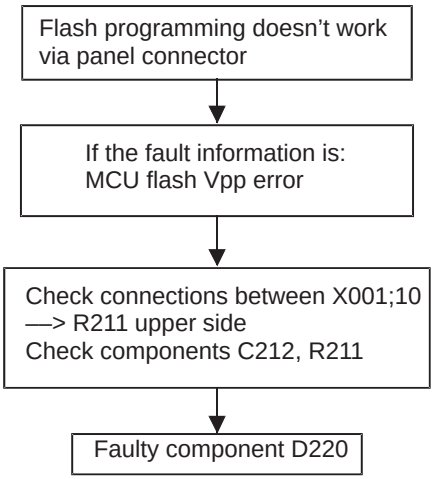


Flash Programming failure (1)

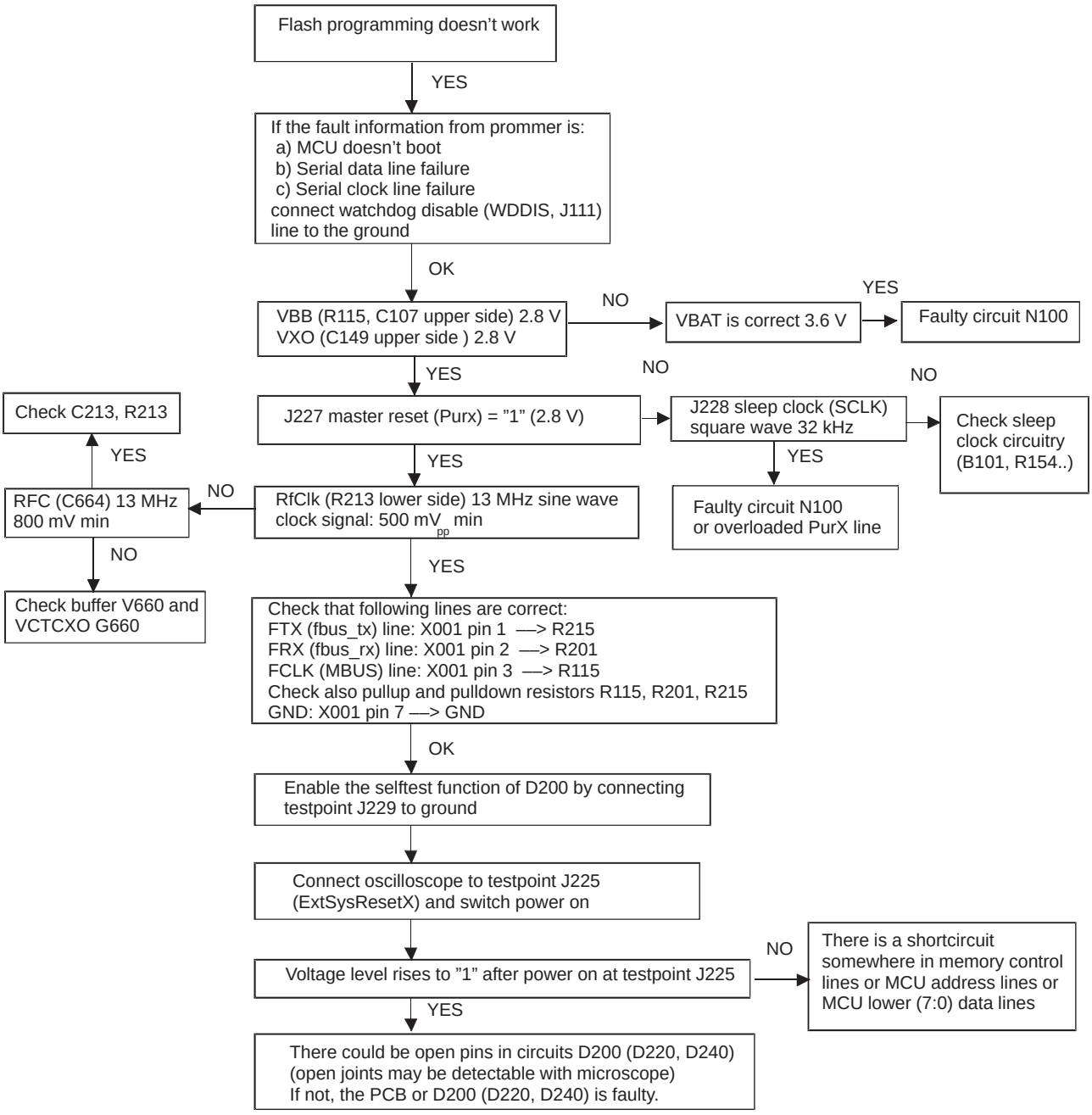


Flash Programming failure (2)

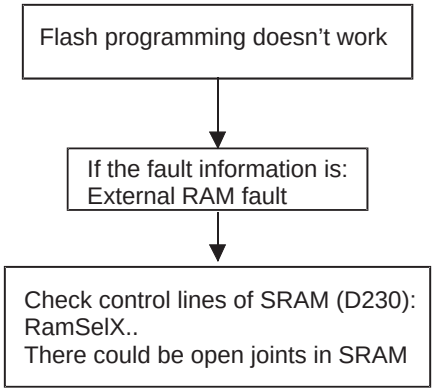


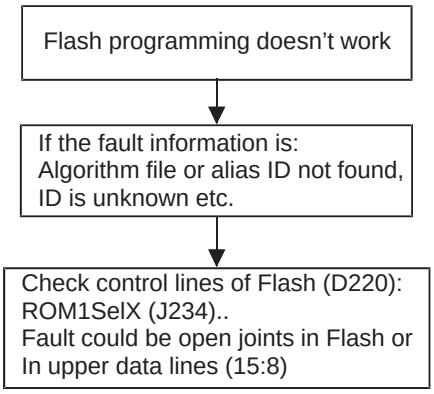


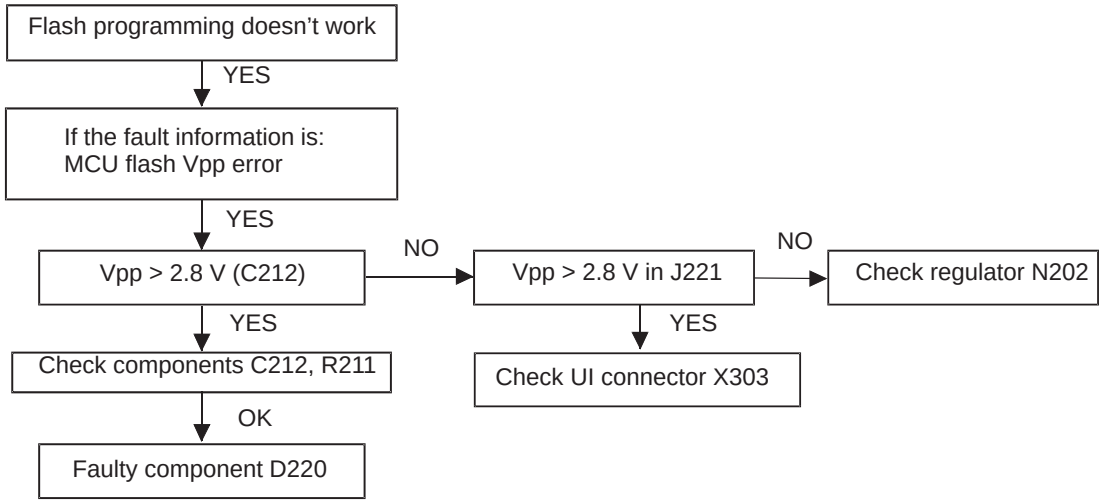
Flash Programming failure (3)



Flash Programming failure (4)



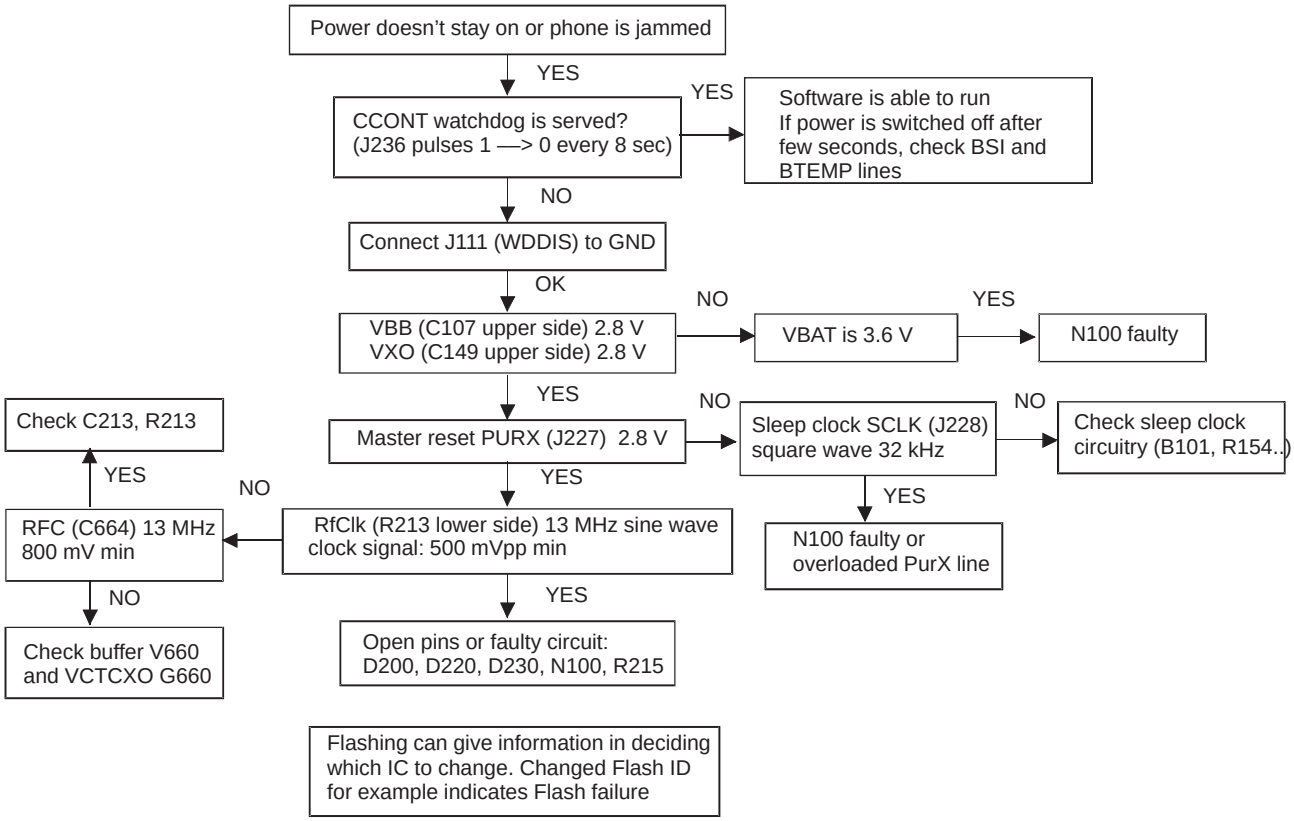




Power doesn’t stay on, or phone is jammed

If this kind of fault has come after flash programming, there are most probably open joints in ICs. The solder joints of ICs: MAD2 (D200), Flash (D220) and SRAM (D230) are to be checked at the extent possible (by microscope from the side of PCB and lightly pressing components while switching power on).

Normally the power will be switched off by CCONT (N100) after 30 seconds if the watchdog of the CCONT can not be served by software. This updating can be seen with an oscilloscope at CCONTCSX (J236). In normal case there is a short pulse from “1” to “0” every 8 seconds. The power off function can be prevented by connecting WDDIS (J111) to ground.



Display Information: Contact Service

This fault means that software is able to run and thus the watchdog of CCONT (N100) can be served. Selftest functions are run when power is switched on and software is executed from flash. If any of the selftests fails, a “contact service” text is shown on display.

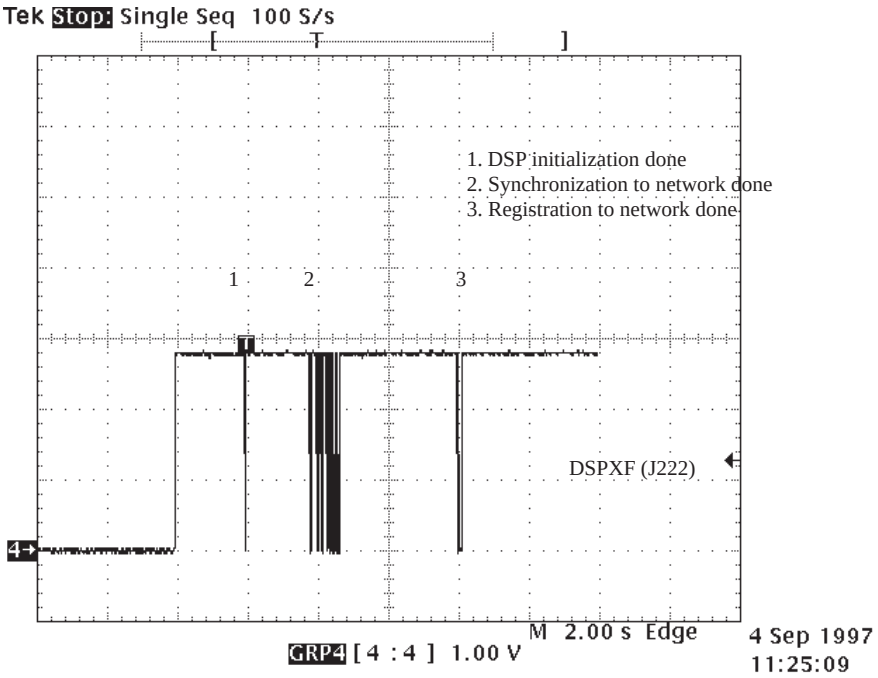
MCU self tests are devided to those executed while power up (start up tests) and ones that can be executed with connected PC. The tests and included items are as follows:

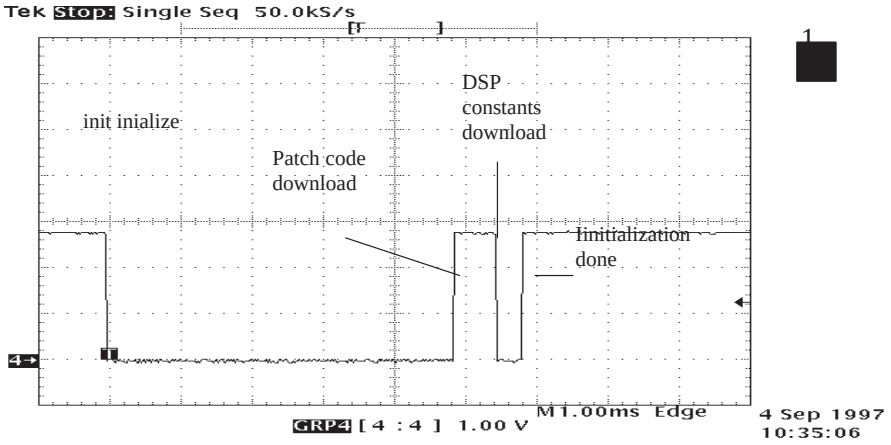
1. MCU ROM checksum
Calculates 16 bit checksum out of Flash code and compares it to one found in Flash. Items being checked are:
MAD2 <—> Flash data– and address lines, CE0,CE1, WE, BYTE, Vcc, GND, Flash internal functionality
2. MCU RAM interface
3. MCU RAM component
4. MCU EEPROM interface
5. MCU EEPROM component
6. RTC battery
7. CCONT interface
8. A/D converter
9. SW reset
A Power off
B. Security data
C. EEPROM tune checksum
D. PPM checksum
E MCU download DSP
F. DSP alive
G. COBBA serial
H COBBA parallel
I. EEPROM sec checksum
K. PPM validity

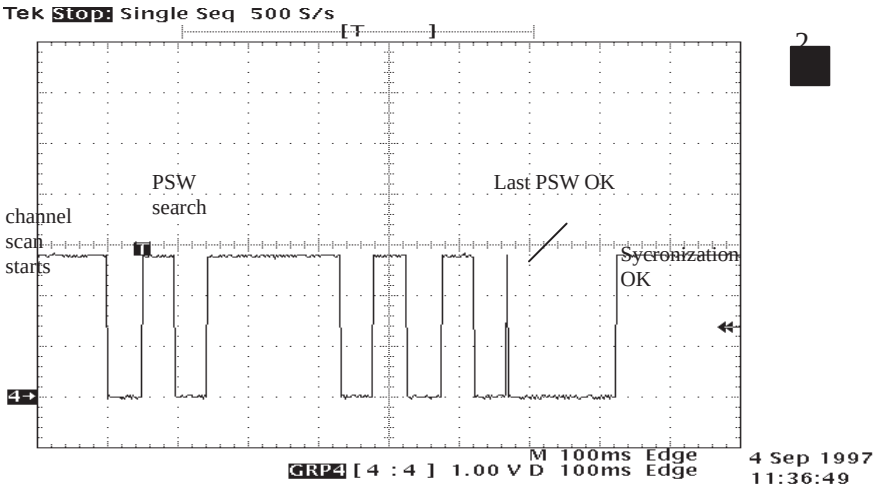
The phone doesn’t register to the network or phone doesn’t make a call

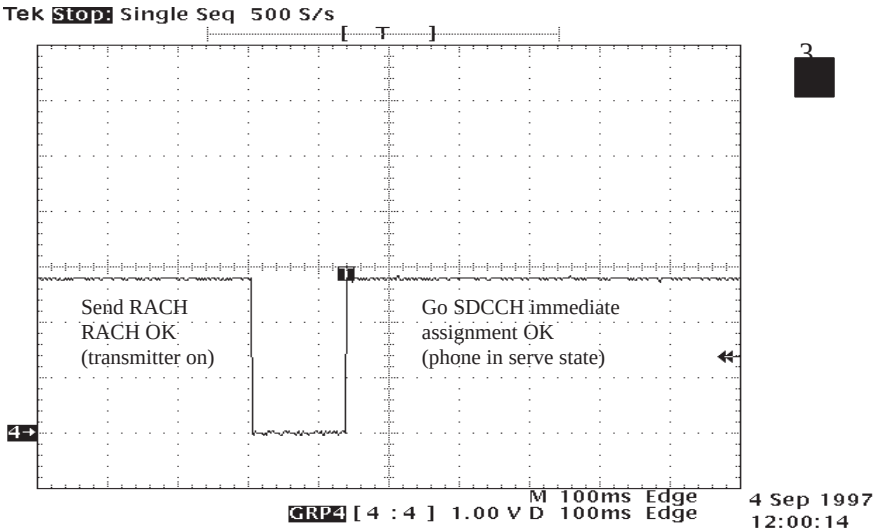
If the phone doesn’t register to the network or the phone doesn’t make a call, the reason could be either on baseband or RF. The phone can be set to wanted mode with WinTesla service software in order to find out whether the fault is in RF or in baseband (RF interface measurements).

The control lines for RF are supplied both by the System Asic (inside of MAD2;D200) and the RFI (inside of Cobba; N250). MAD2 handles digital control lines (like SENA, TxP etc.) and Cobba handles analog control lines (like AFC, TxC etc.). The DSP software is constructed so that operation states of DSP (MAD2) can be seen in external flag, DSPXF (J222). After power up, DSP will signal all the completed functions by changing the state of the XF pin.

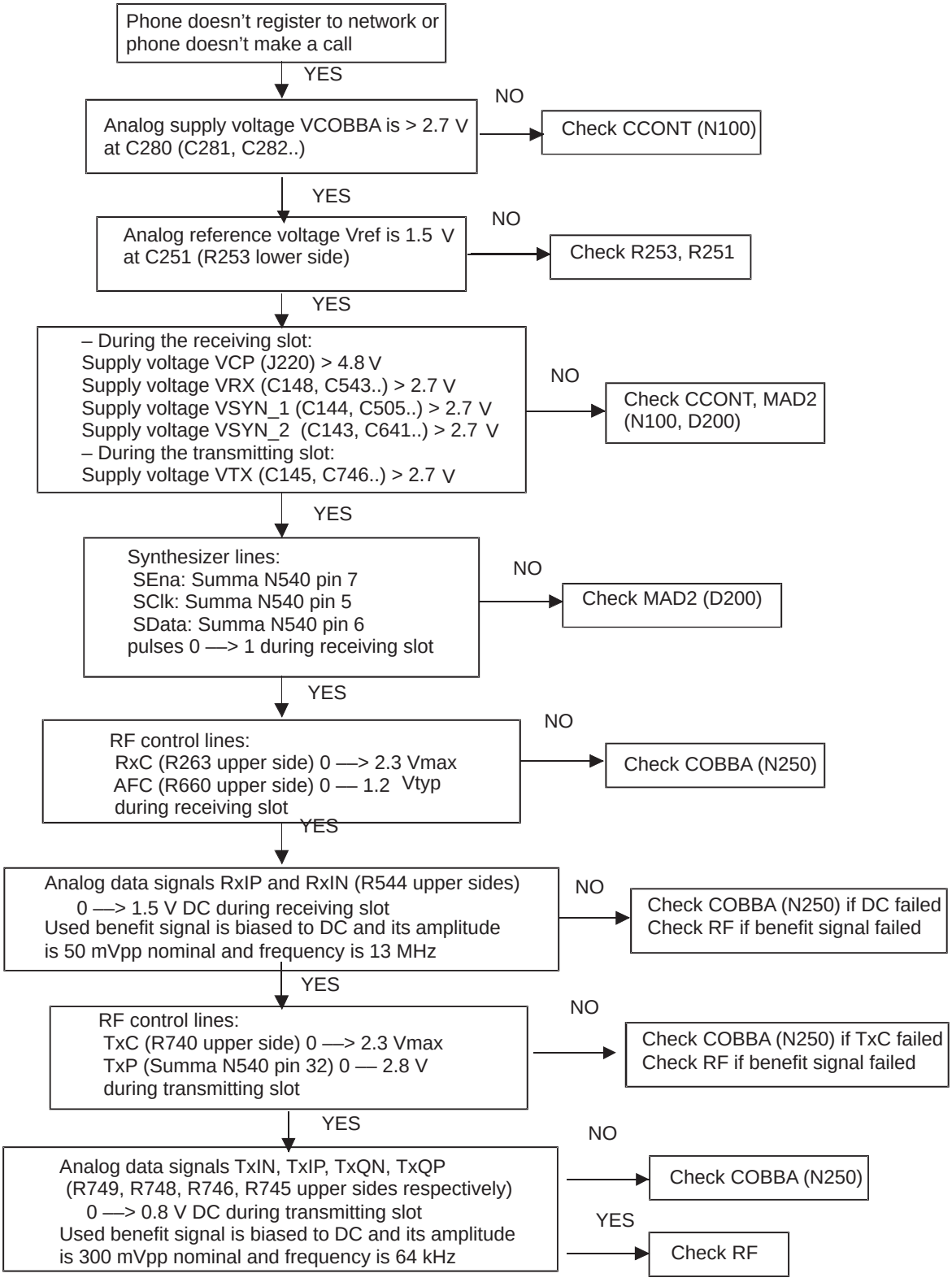



Tek Stop: Single Seq 50.0kS/s
1
init inialize
Patch code
download
DSP
constants
download
Initialization
done
M1.00ms Edge
GRP4 [4 :4] 1.00 V
4 Sep 1997
10:35:06


Tek Stop: Single Seq 500 S/s
2
PSW
search
Last PSW OK
channel
scan
starts
Sycronization
OK
M 100ms Edge
GRP4 [4 :4] 1.00 V D 100ms Edge
4 Sep 1997
11:36:49


Tek Stop: Single Seq 500 S/s
3
Send RACH
RACH OK
(transmitter on)
Go SDCCH immediate
assignment OK
(phone in serve state)
M 100ms Edge
GRP4 [4 :4] 1.00 V D 100ms Edge
4 Sep 1997
12:00:14

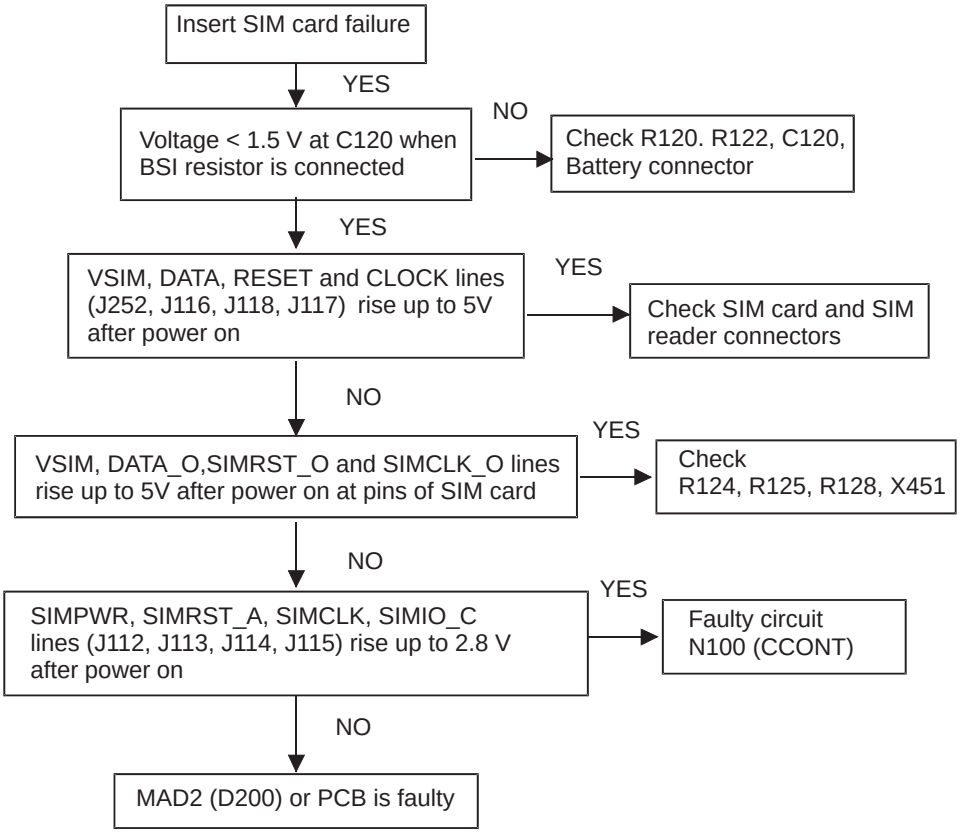
Phone register failure



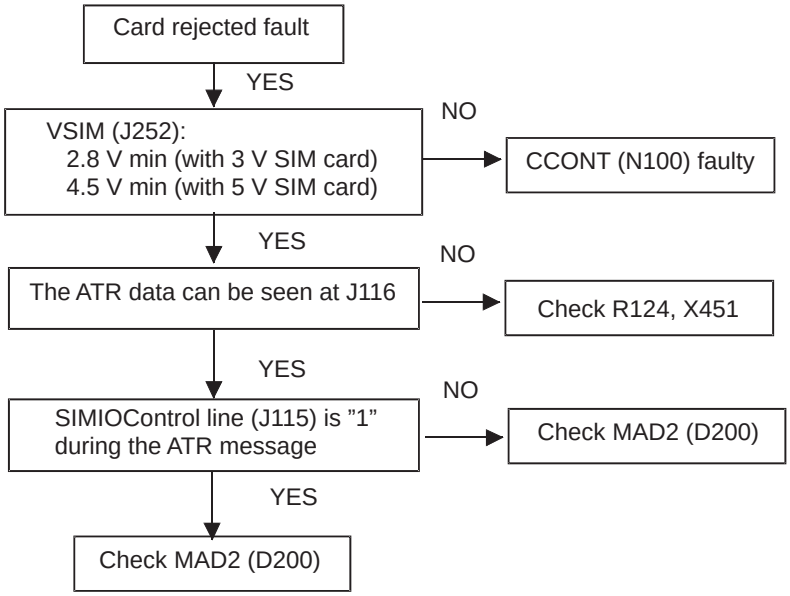
SIM card related failures

The hardware of the SIM interface from MAD2 (D200) to the SIM connector (X451) can be tested without a SIM card. When the power is switched on and the BSI line (J122) is grounded by a resistor, all the used lines (VSIM, RST, CLK, DATA) rise up to 5 V four times. Thus “Insert SIM card” faults can be found without SIM card.

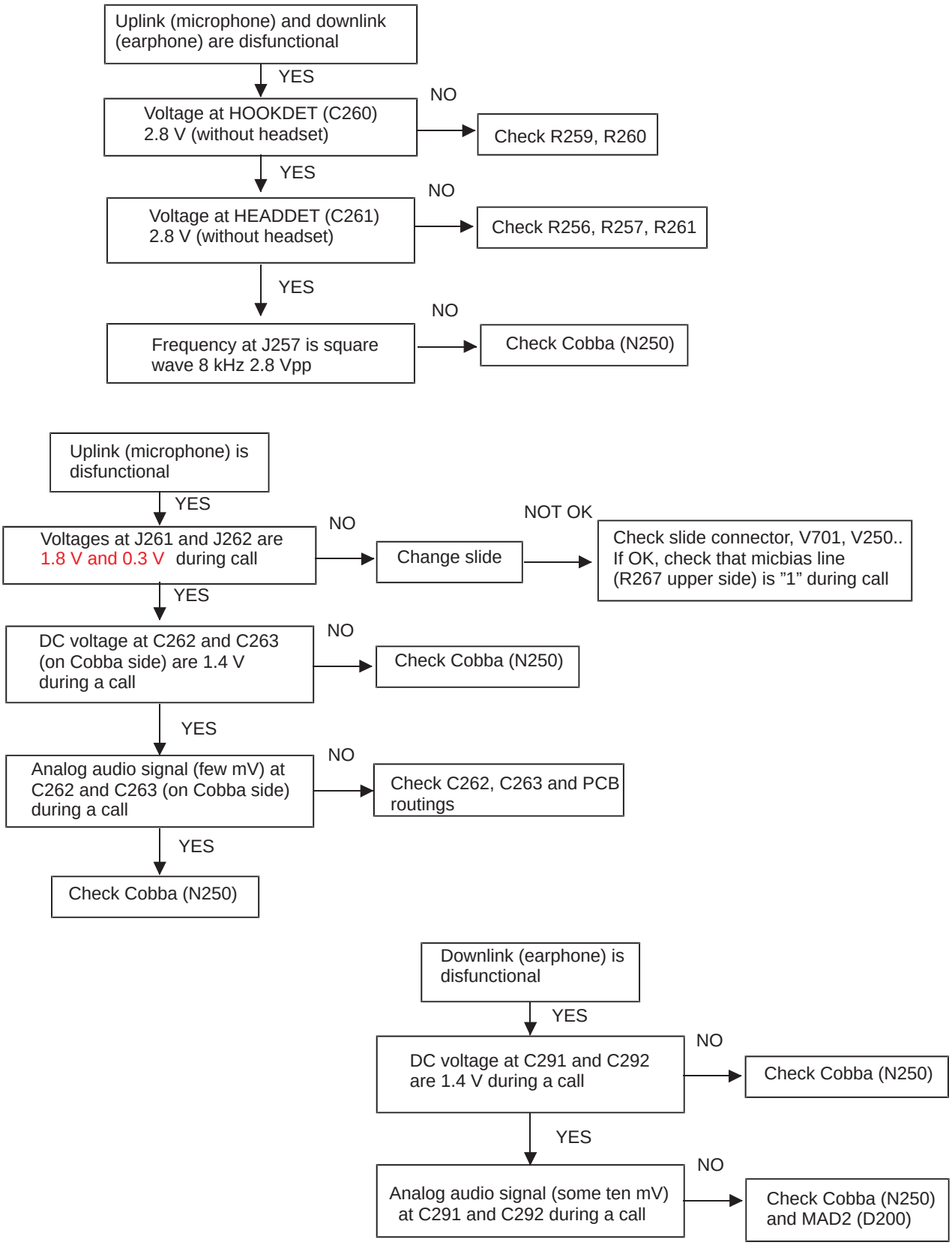
The fault information “Card rejected” indicates that ATR message (the first message is always sent from card to the phone) is sent from card but the message is somehow corrupted, data signal levels are wrong etc. or factory set values (stored to the EEPROM) are not correct.



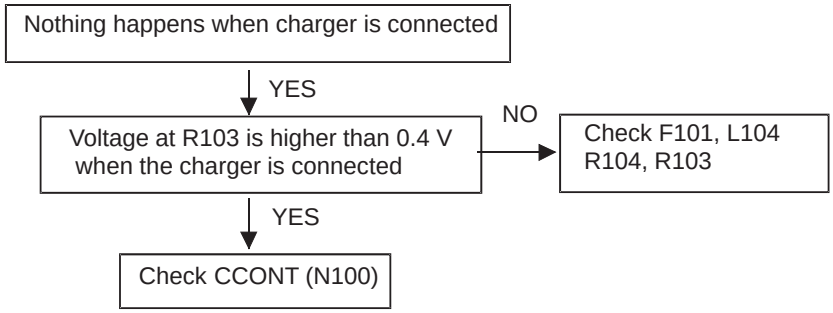
SIM Card failure

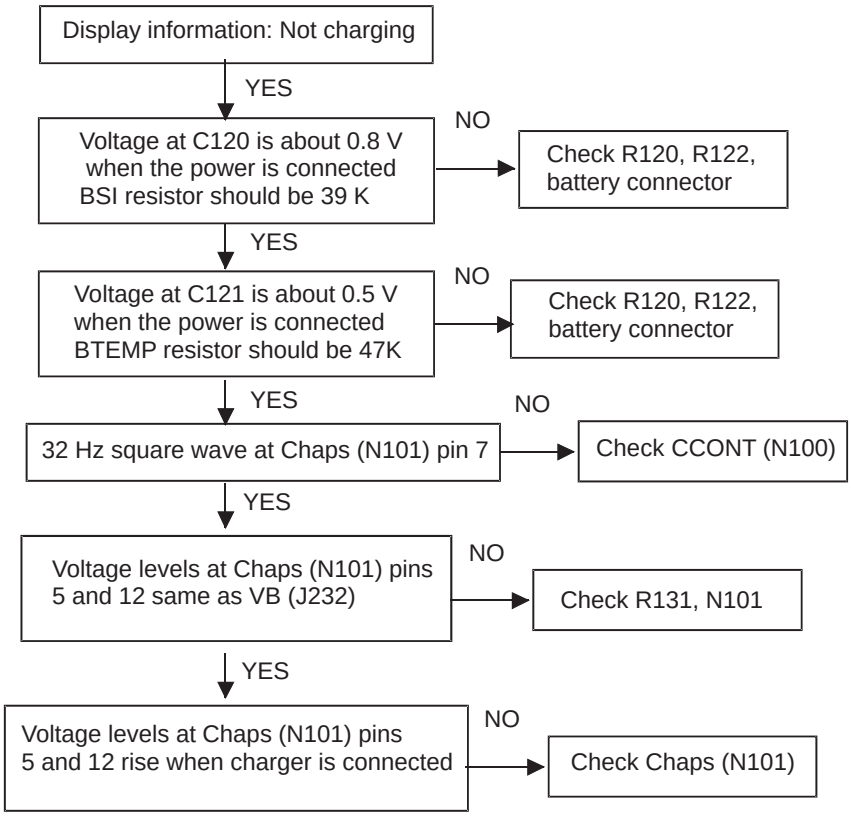


Audio failure

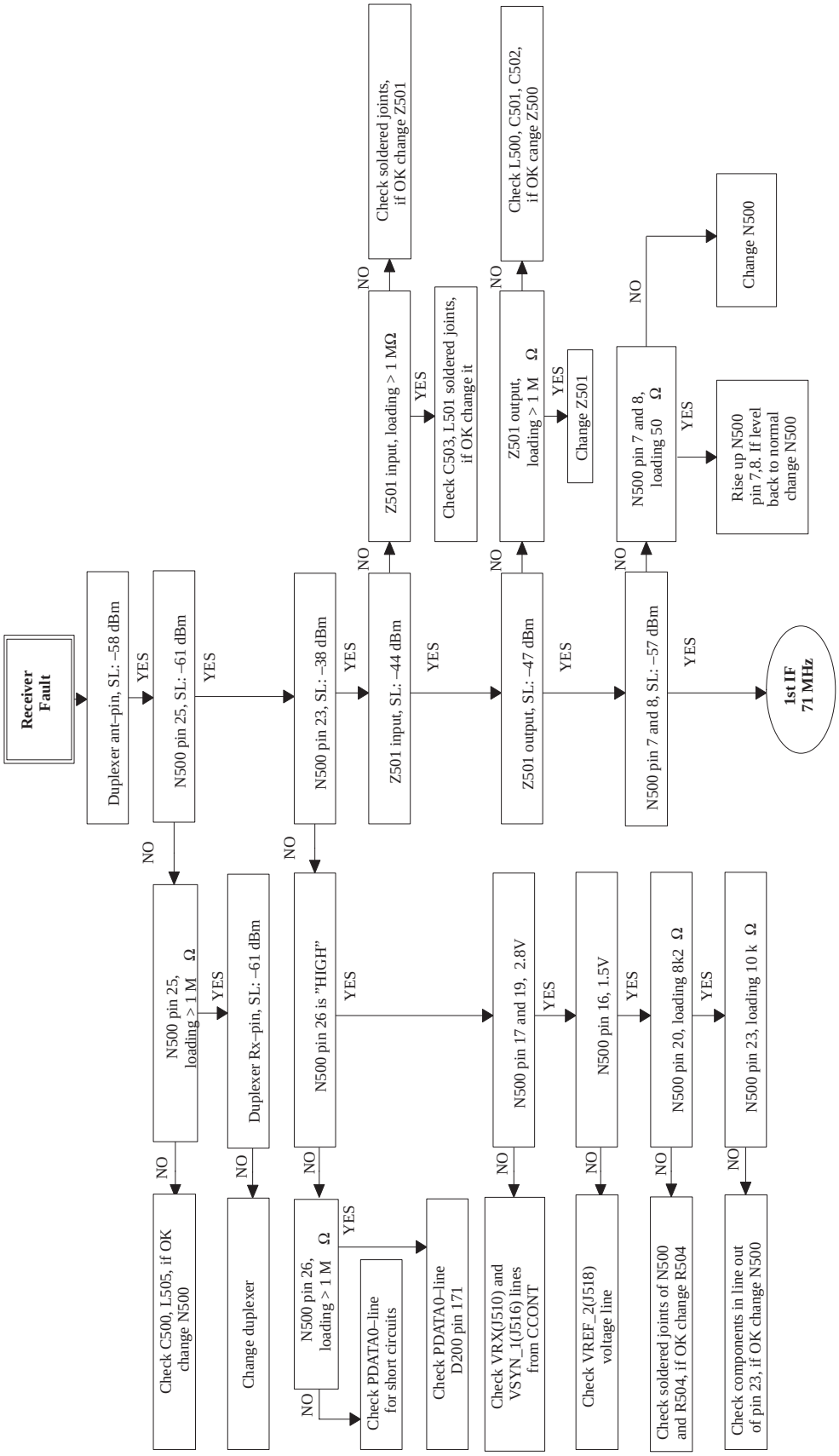


Charger failure

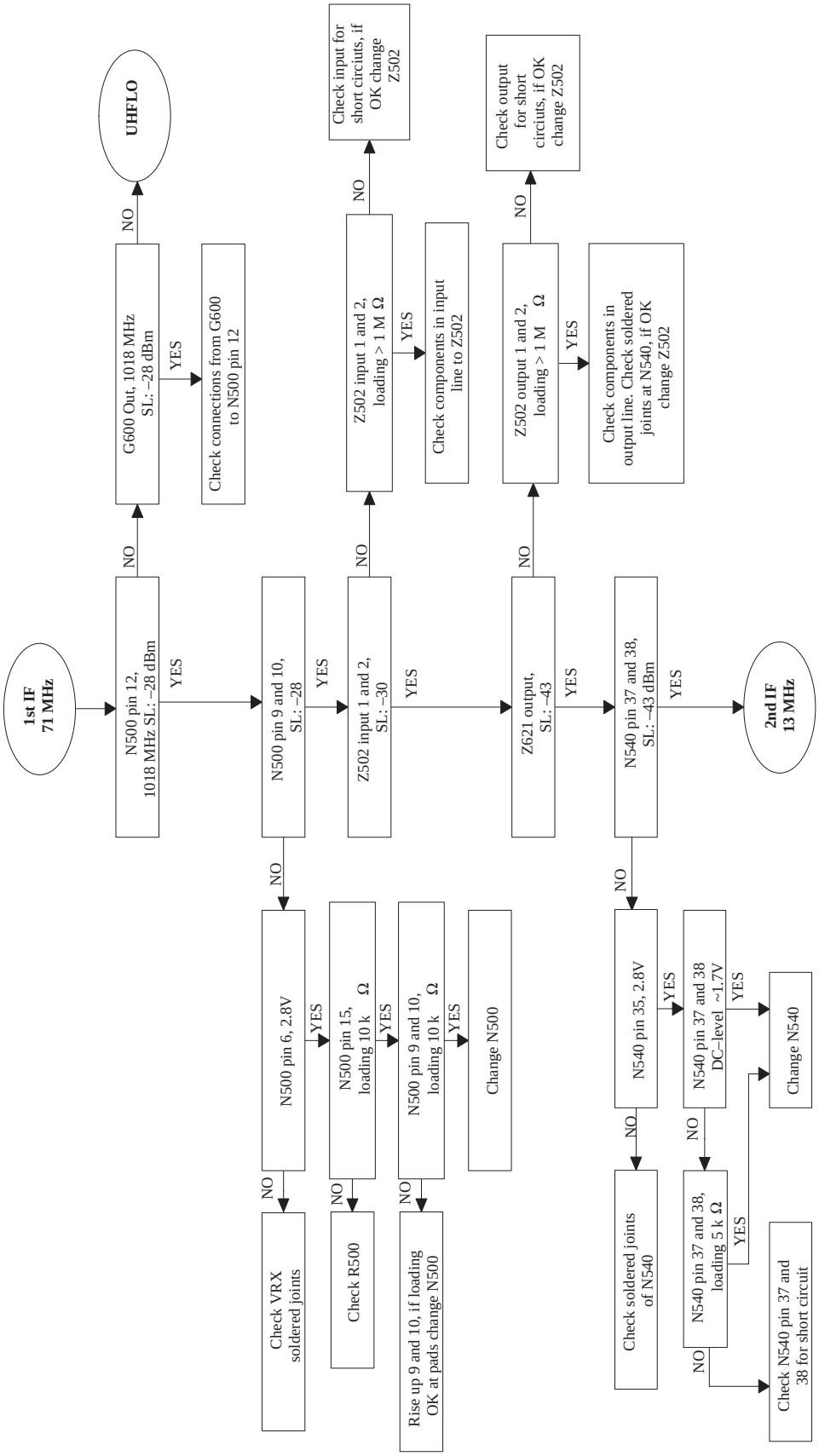




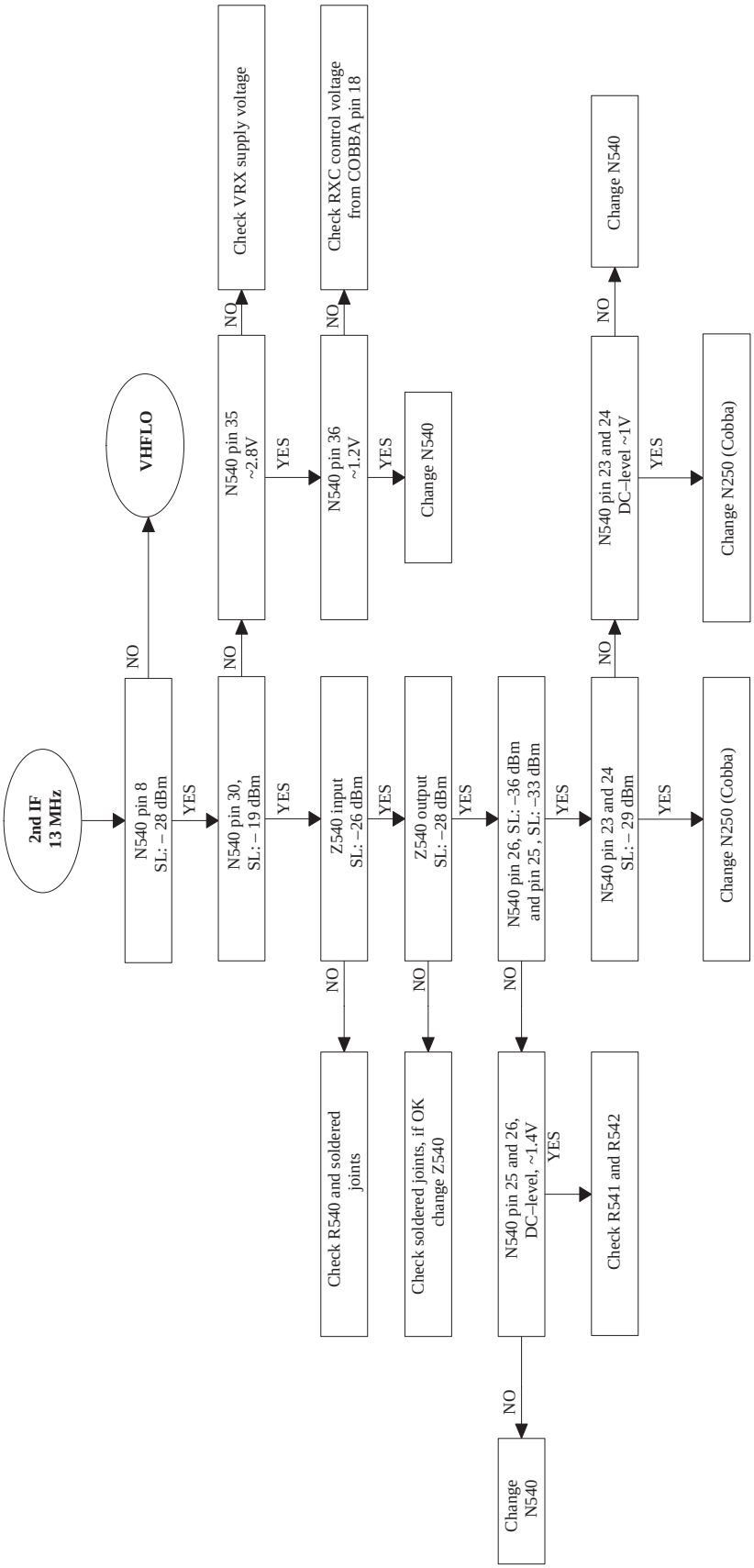
Receiver Fault (1)



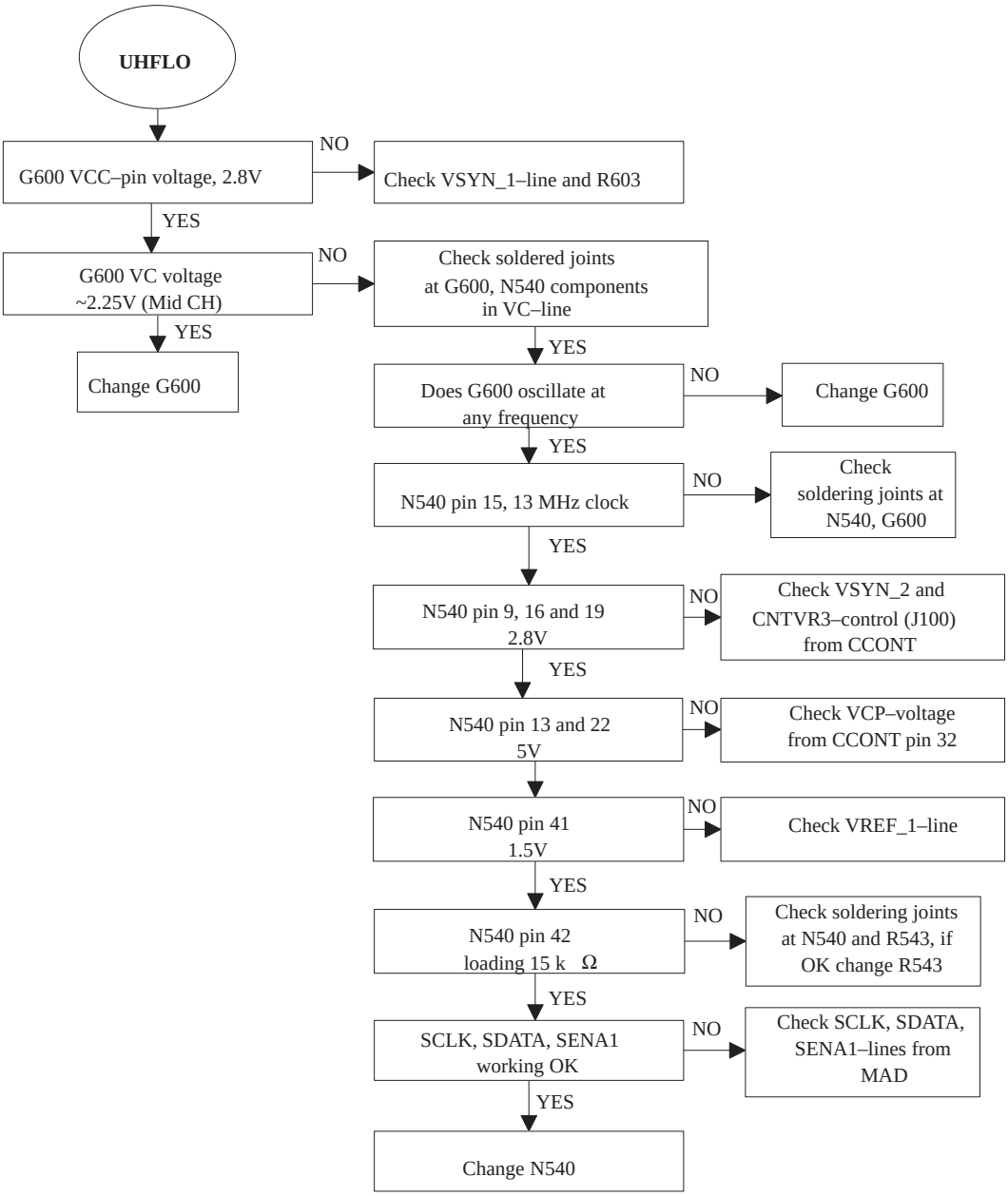
Receiver Fault (2)



Receiver Fault (3)

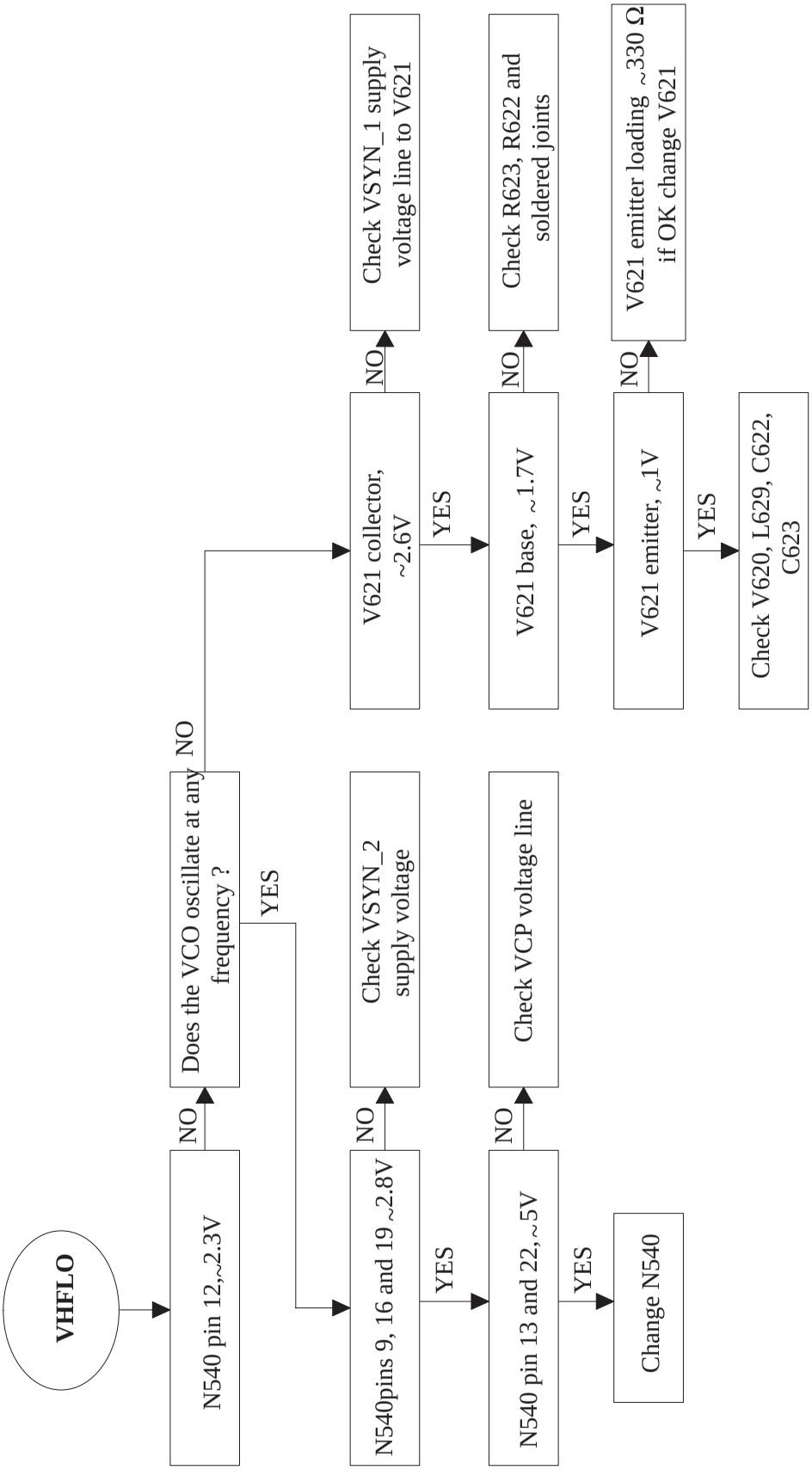


Receiver Fault (4)

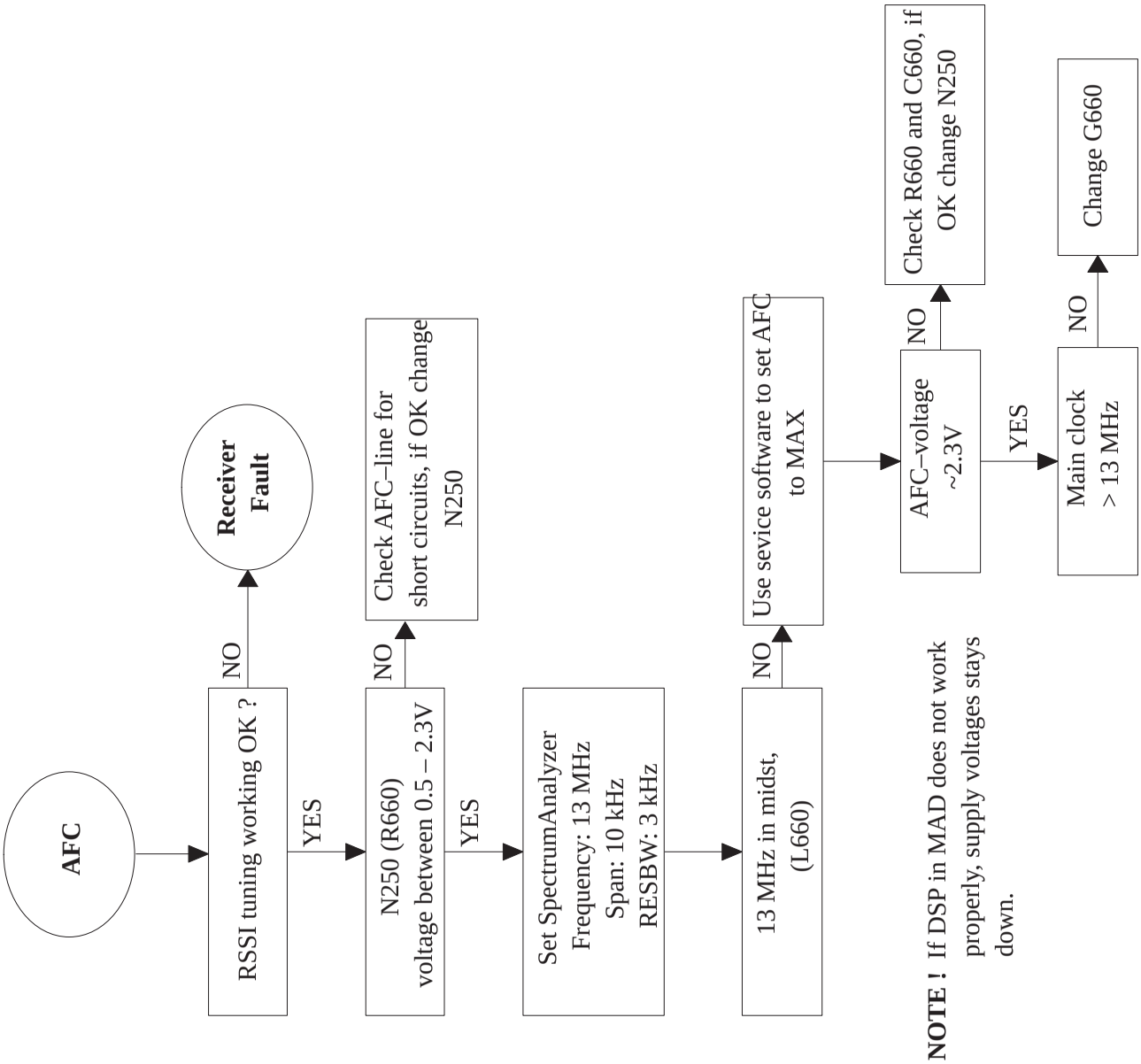


13 MHz clock oscilloscope picture in Appendix A
SCLK, SDATA, SENA1 oscilloscope pictures in Appendix B

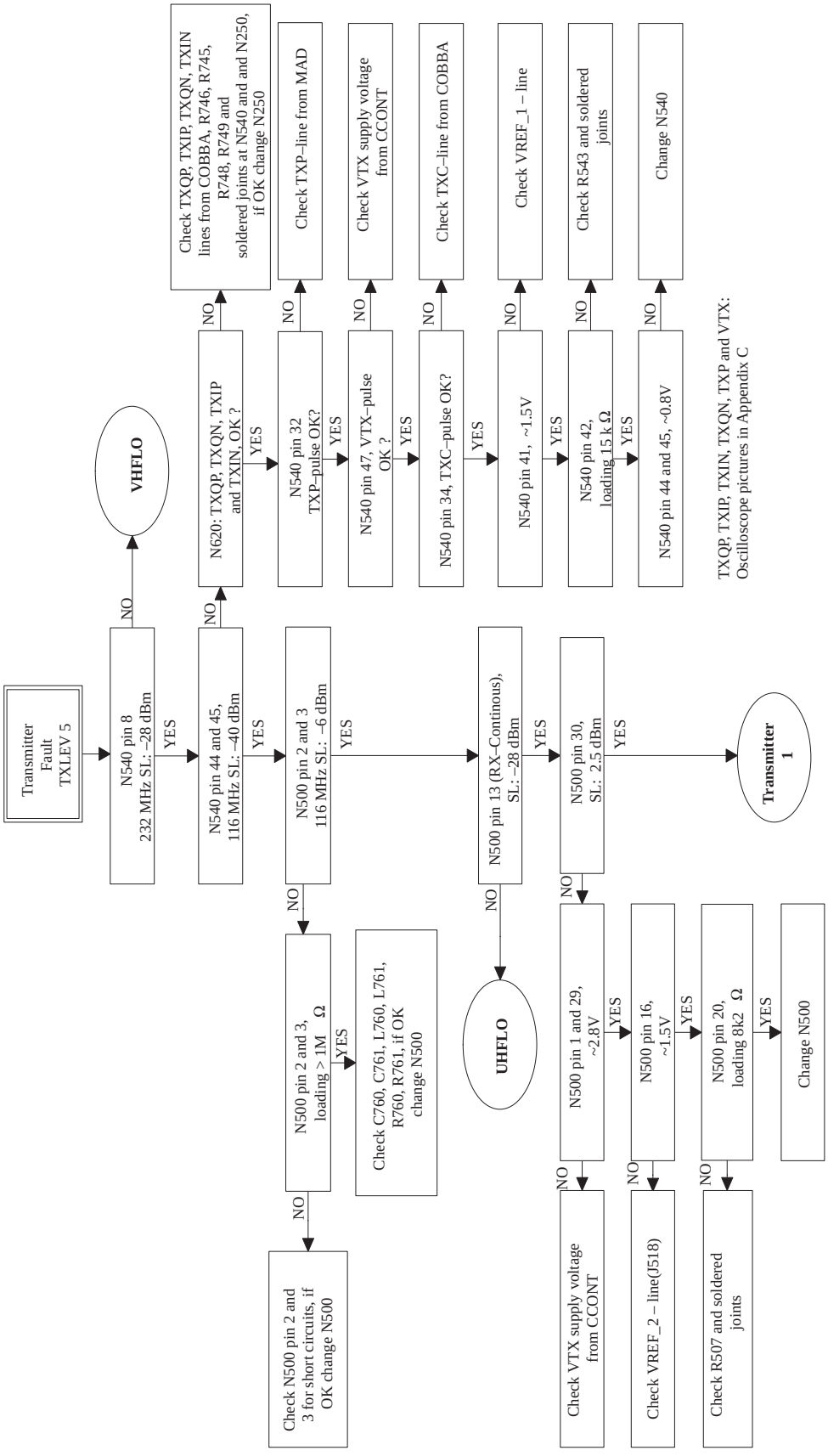
Receiver Fault (5)



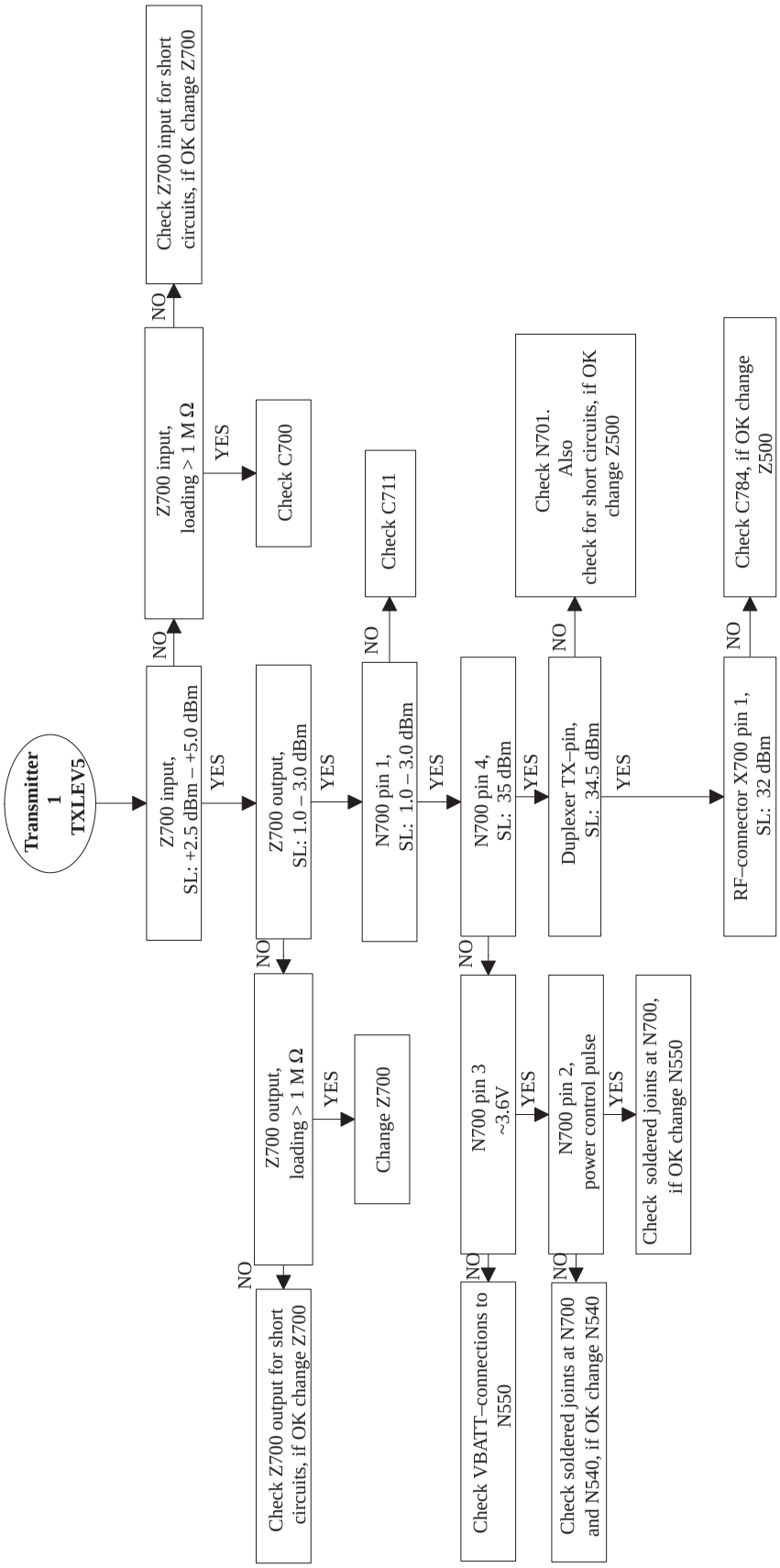
Receiver Fault (6)



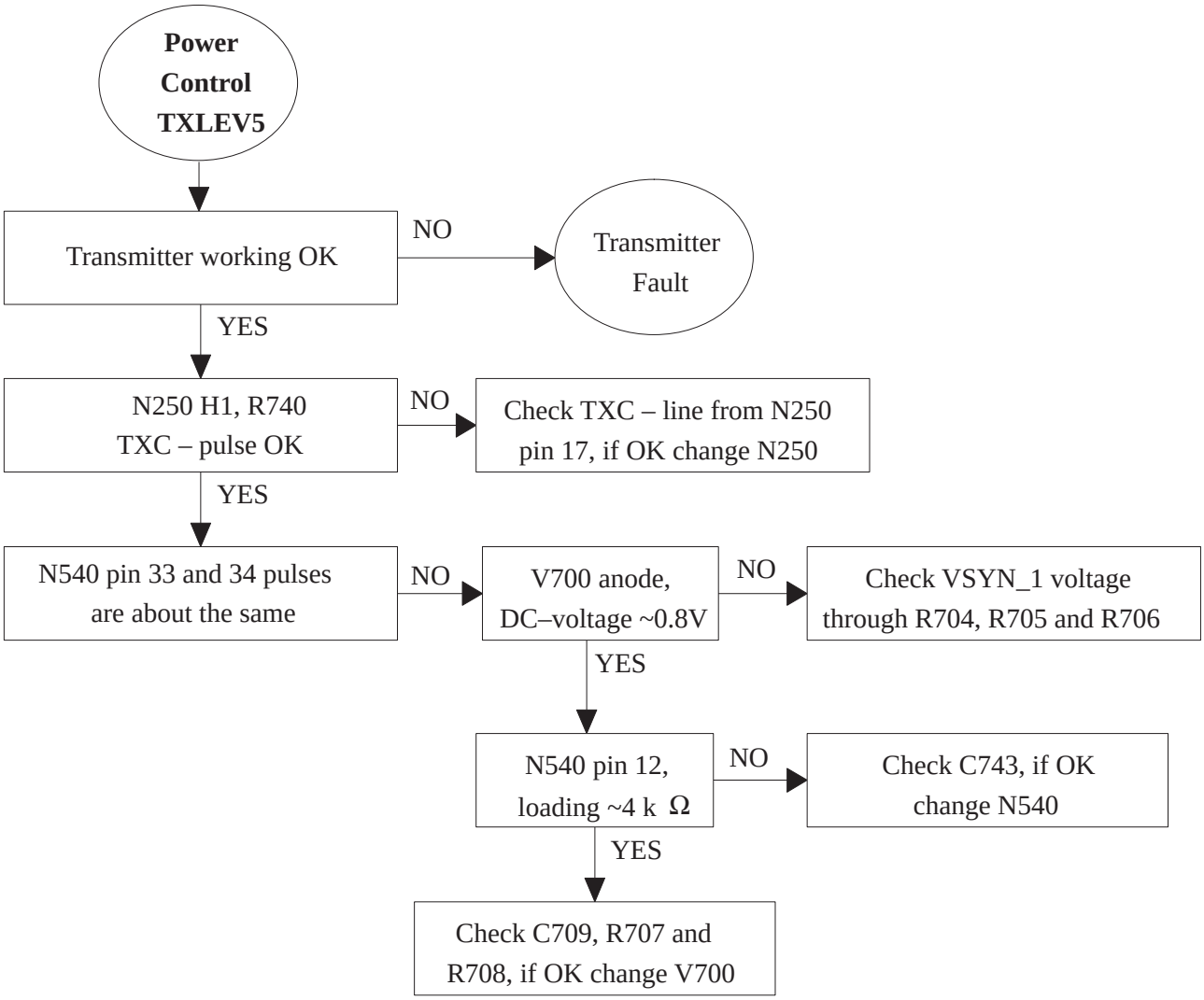
Transmitter Fault (1)



Transmitter Fault (2)

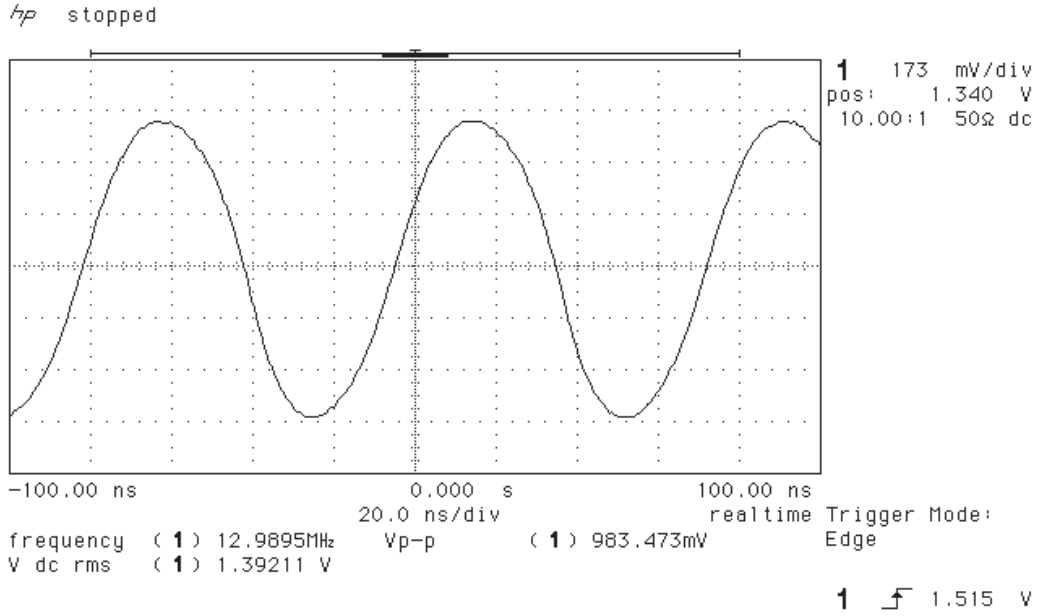


Transmitter Fault (3)



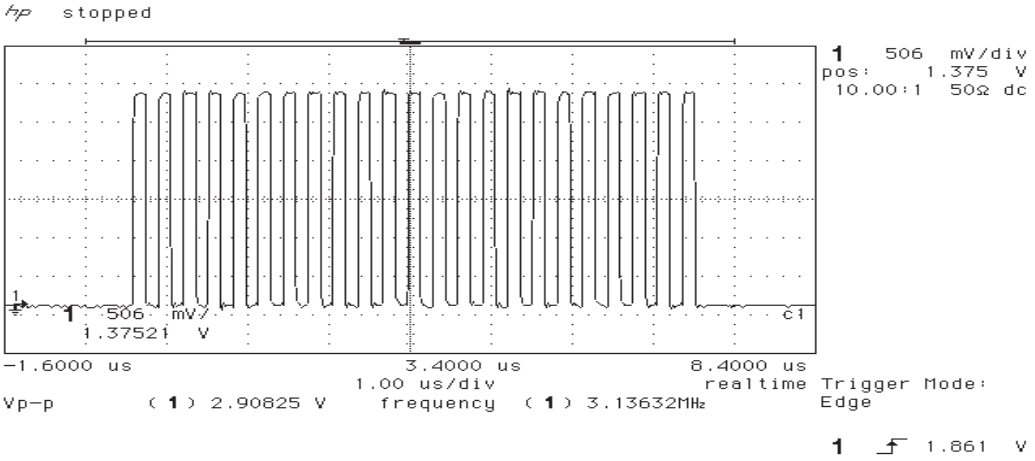
TXC – pulse:
Oscilloscope picture in Appendix D

Appendix A

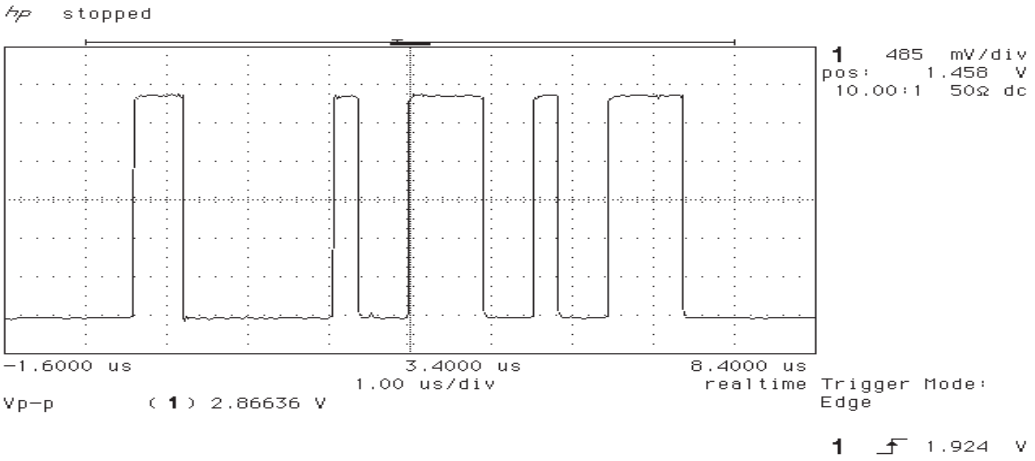


Picture 1. 13 MHz Main clock – signal

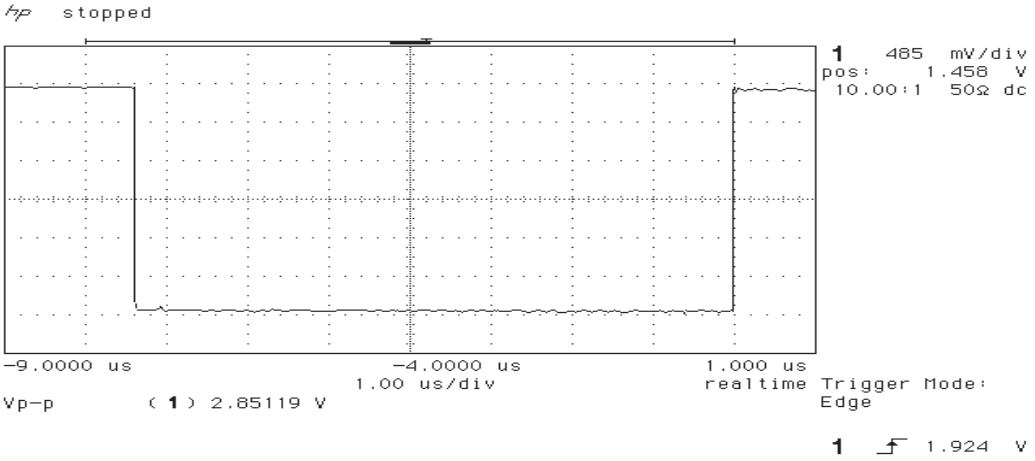
Appendix B



Picture 2. SCLK – signal

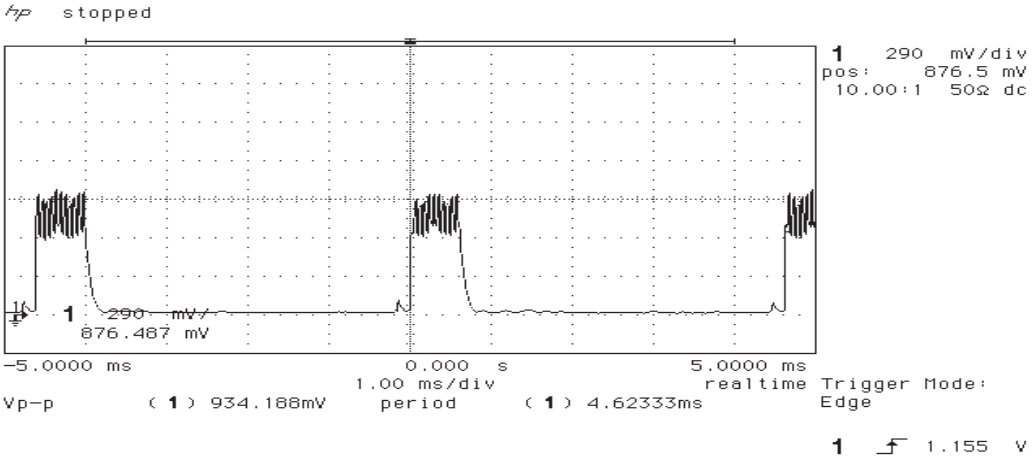


Picture 3. SDATA – signal

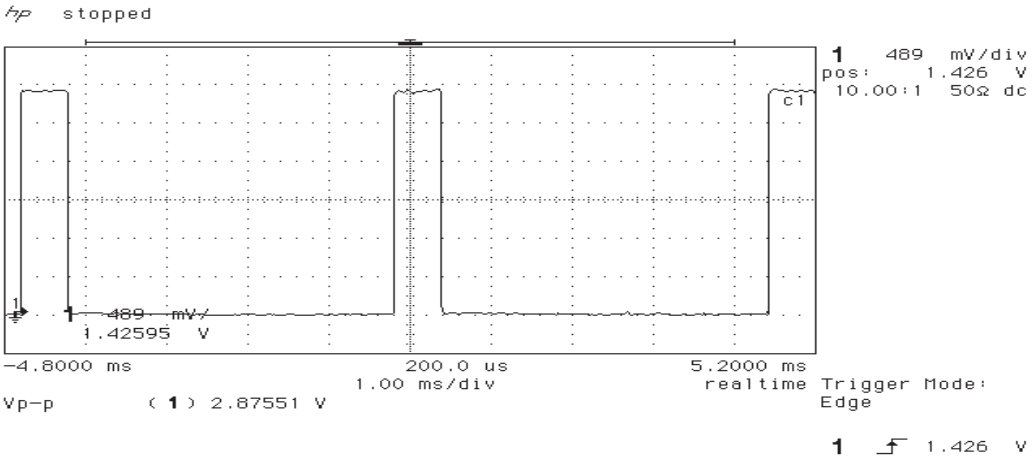


Picture 4. SENA1 – signal

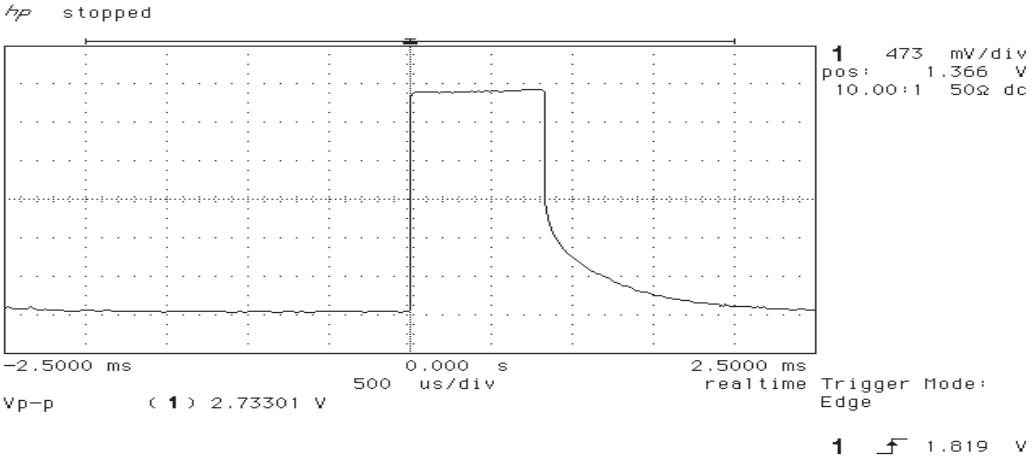
Appendix C



Picture 5. TXQP, TXQN, TXIP and TXIN – signal

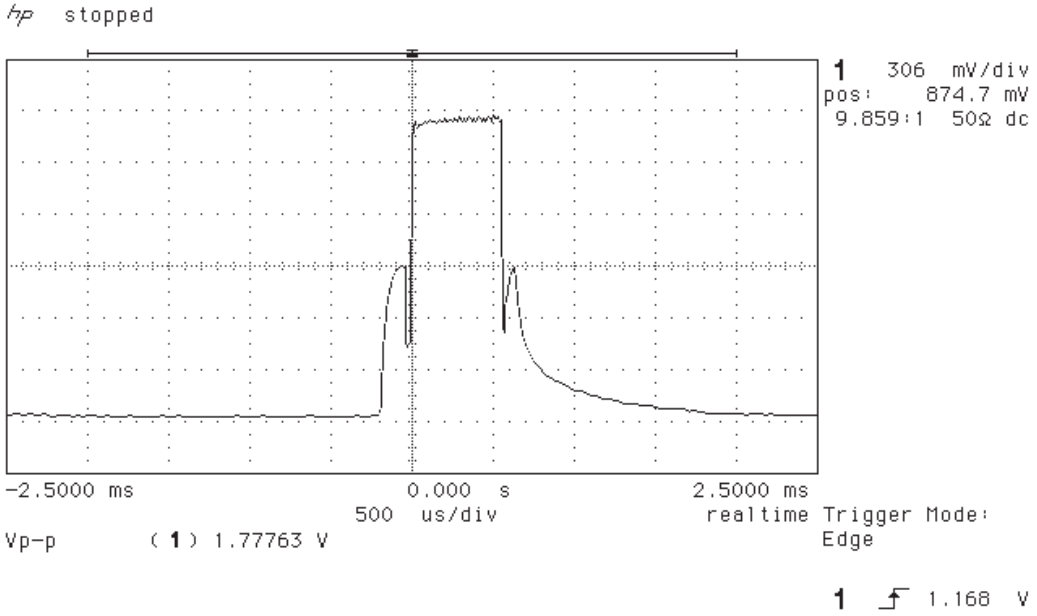


Picture 6. TXP – signal

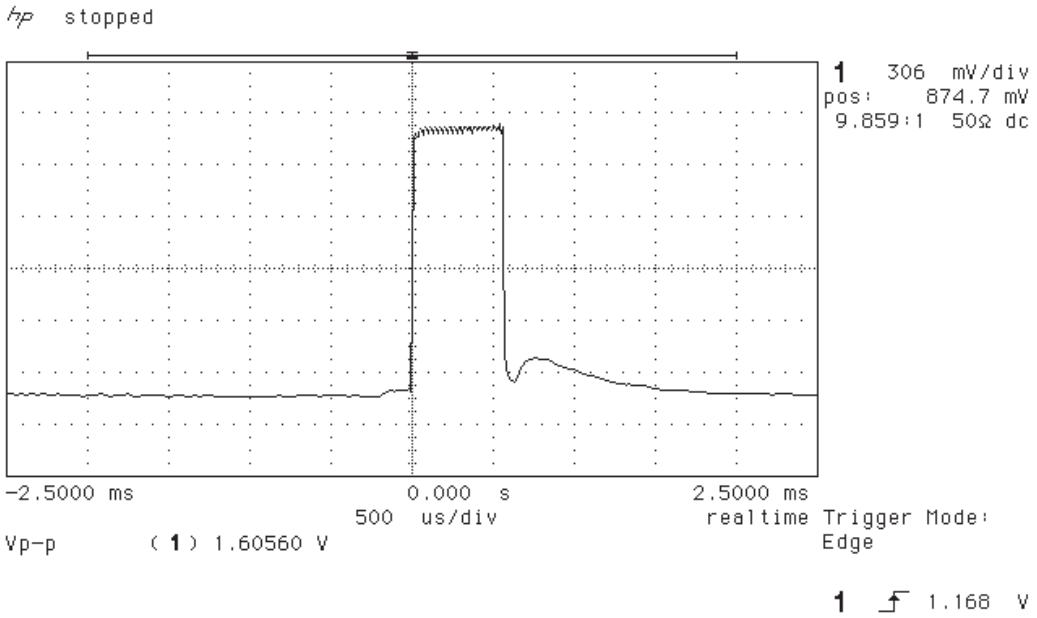


Picture 7. VTX – signal

Appendix D



Picture 8. TXC – signal (TXLEV5)



Picture 9. DET – signal(N620 pin 12) TXLEV5

Test points

Test Point	Name	Logic Level	Min	Max	Unit	Description
J100	SYNTHP	0 1	0 2.0	0.8 2.85	V	Control line for VSYN_1 and VSYN_2.
J101	SLEEPX	0 1	0 2.0	0.5 2.85	V	Control line for VCXO module supply. If low, 13 MHz clock is disabled.
J102	TXPWR	0 1	0 2.0	0.5 2.85	V	Control line for VTX voltage
J103	RXPWR	0 1	0 2.0	0.5 2.85	V	Control line for VRX voltage
J107	L_GND		0	0	V	Charger ground
J108	CHRG_CTRL	0 1	0 2.0	0.8 2.85	V	Charger control for external charger. 1 Hz for stand– by charging, 32 Hz for continuous charging.
J109	VIN		0	15	Vpeak	Charging voltage
J110	VPP		2.8	3.2	V	Supply voltage for flash programming (Vpp). Vpp will be switched on only during flash programming.
J111	WDDIS			5.3	V	Power is forced to stay on when WDDIS is grounded (watchdog disable)
J112	SIM_PWR	0 1	0 2.0	0.8 2.85	V	Control line for SIM voltage supply.
J113	SIMRST_A	0 1	0 2.0	0.8 2.85	V	Control line for SIM reset
J114	SIMCLK	0 1	0 2.0	0.8 2.85	V	Clock to SIM interface (3.25MHz, MAD2 side of CCONT)
J115	SIM I/O_C	0 1	0 2.0	0.8 2.85	V	SIM data on MAD2 side of CCONT
J116	DATA_O	0 1	0 2.8/4.0	0.5 3.2/5.2	V	SIM data in SIM contacts

J117	SIMCLK_O	0 1	0 2.0	0.8 2.85	V	Clock line to Sim (3.25MHz)
J118	SIMRST_O	0 1	0 2.8/4.0	0.5 3.2/5.2	V	Sim reset line
J119	VCOBBA		2.7	2.85	V	Supply voltage for analog part of COBBA
J153	GND		0	0	V	
J154	MBUS	0 1	0 2.0	0.8 2.85	V	Data I/O for external device and clock signal from flash prommer to MAD2
J220	V5V		4.8	5.2	V	Supply voltage for RF circuits. (VCP)
J221	5V		2.8	3.2	V	Supply voltage for flash programming (Vpp). Vpp will be switched on only during flash programming.
J222	DSPXF	0 1	0 2.0	0.8 2.85	V	Test point for fault diagnostic.
J223	CCONTINT	0 1	0 2.0	0.8 2.85	V	Interrupt line from CCONT to MAD2. Used for charger indication and RTC alarm indication. If high, an interrupt is generated.
J224	VSRM		5.2	5.5	V	Supply voltage for flash programming regulator N201 from CCONT (N100)
J225	EXTSYSRESETX	0 1	0 2.0	0.8 2.85	V V	Testpoint for fault diagnostic. If missing, check power supply, PurX line and 13 MHz clock signal.
J226	EXTSYSRESETX	0 1	0 2.0	0.8 2.85	V	Testpoint for fault diagnostic. If missing, check power supply, PurX line and 13 MHz clock signal.
J227	PurX	0 1	0 2.0	0.8 2.85	V	Power up reset line from CCONT to MAD. If low, the bb circuits are in reset state.
J228	SLEEPCLK	0 1	0 2.0	0.8 2.85	V	32 kHz square wave clock from CCONT to MAD.
J229	SELF TEST	0 1	0 2.0	0.8 2.85	V	Self test pin. If short–circuit is made between testpoint J229 and J230, the self test will be executed.
J230	GND		0	0	V	

J231	MCURDX	0 1	0 2.0	0.5 2.85	V	MCU read strobe
J232	VB		3.0	5.3	V	Battery voltage
J233	MCUWRX	0 1	0 2.0	0.5 2.85	V	MCU write strobe
J234	ROM1SELX	0 1	0 2.0	0.5 2.85	V	Flash memory select
J235	RAMSELX	0 1	0 2.0	0.5 2.85	V	Sram memory select
J236	CCONCSX	0 1	0 2.0	0.8 2.85	V	Chip select for CCONT from MAD2. Active low. Pulses 1—>0 every 8 sec, if software is running
J250	GND		0	0	V	
J251	AGND		0	0	V	
J252	VSIM	(5V) (3V)	4.8 2.8	5.2 3.2	V	SIM supply voltage
J253	VSRM		5.2	5.5	V	Supply voltage for flash programming regulator N201 from CCONT (N100)
J254	SGND		0	0	V	
J254	–					
J255	FBUS_RX	0 1	0 2.0	0.8 2.85	V	Data input from external device, data from IR to MCU module, and data from flash prommer to MCU.
J256	FBUS_TX	0 1	0 2.0	0.5 2.85	V	Data output for external device, data from MCU to IR module, and data to flash prommer.
J257	8KHZ	0 1	0 2.15	0.5 2.85	V	8 KHz frame sync
J261	MICP			4.1	mV	Internal microphone positive pole
J262	MICN			4.1	mV	Internal microphone negative pole
J780	(VDDTXMIX)					
	VBB		2.7	2.85	V	Baseband main voiltage
	VXO		2.7	2.85	V	VCTCXO voltage (13 MHz clock)
	RFCLK		0.5		Vpp	13 Mhz clock for baseband and RF

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